


Security Classification		LC Future Center Secret Data	
Issued Date	2013/09/07	Deciphered Date	2014/09/07
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Title			
<b>BLOCK DIAGRAM</b>			
Size	Document Number	Rev 1.0	
Custom	<b>BE460 NM-A551</b>		
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Voltage Rails ( O --> Means ON , X --> Means OFF )

Power Plane State	B+	+1VALW +1.8VALW +3VALW +5VALW	+1.35V	+5VS +3VS +0.675VS +VCC_CORE +VGA_CORE +3VS_VGA +1.8VS_VGA +1.35VS_VGA +1VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON	SUSP#
S0		HIGH	HIGH	HIGH	HIGH	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF

USB2 Port

Port	Device
1	On Board
2	On Board
3	SUB/B
4	ONE-Link DOCK
5	Touch Panel
6	BT
7	CMOS
8	FPR
9	X

USB3 Port

Port	Device
1	On Board
2	On Board
3	SUB/B
4	ONE-Link DOCK

PCIE Port

Port	Device
1	X
2	X
3	WLAN
4	LAN
5	X
6	CardReader
7	X
8	X
9	GPU
10	GPU
11	GPU
12	GPU

SATA Port

Port	Device
1	HDD
2	X
3	X
4	X

SMBUS Control Table

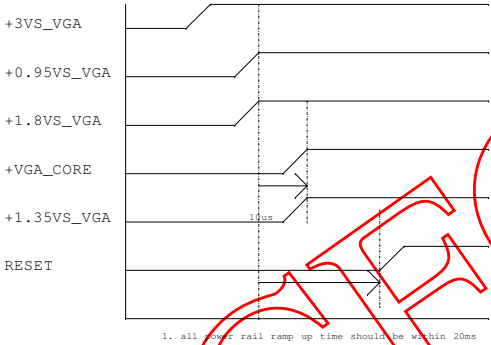
	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Security ROM	LAN PHY	G-Sensor
EC_SMB_CLK1 EC_SMB_DA1	IT8580F +3VL	X	V +3VALW	X	X	X	X	X	X	X	X
EC_SMB_CLK3 EC_SMB_DA3	IT8580F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3VALW_PCH	X	X	X	V +3VALW
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	V +3VS	X	X	X	V +5VS	V +3VS	X	X
PCH_SML0_CLK PCH_SML0_DAT	PCH +3VALW_PCH	X	X	X	X	X	X	X	X	V +3VALW	X

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VGA and DDR3 Voltage Rails (JET TOPAZ GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	N/A	
GPIO5	IN	-	GPIO5_AC_BATT
GPIO6	IN	-	GPIO6
GPIO7	OUT	N/A	
GPIO8	OUT	-	GPIO8_ROMSO
GPIO9	OUT	-	GPIO9_ROMSI
GPIO10	OUT	-	GPIO10_ROMSCK
GPIO11	OUT	N/A	
GPIO12	OUT	N/A	
GPIO13	OUT	N/A	
GPIO15	IN	N/A	SVI2_SVD
GPIO16	OUT	N/A	
GPIO17	OUT	N/A	
GPIO19	OUT	N/A	GPIO19_CTF
GPIO20	IN	IN	SVI2_SVC
GPIO21	OUT	N/A	
GPIO22	OUT	N/A	GPIO22_ROMCSB
GPIO29	OUT	N/A	
GPIO30	OUT	N/A	



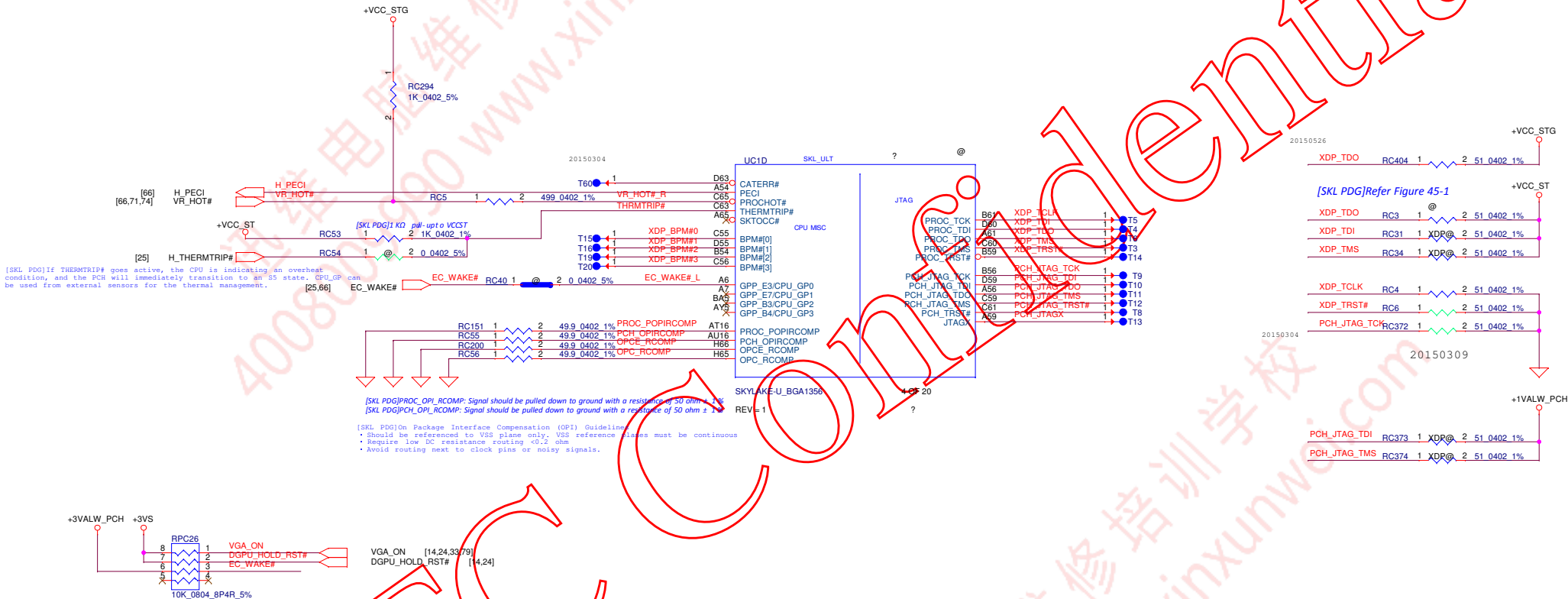
	Device ID
JET-XT	0x6664
TOPAZ XT	0x6900

BOM Structure Table

BOM Structure	NOTE
EXO@	For GPU_EXO
MESO@	For GPU_MESO
DIS@	For GPU function
X76@	GPU VRAM Setting
TPM@	Trusted Platform Module (TPM)
DIMM1@	JDIMM1 function
DIMM2@	JDIMM2 function
UMA@	UMA SKU ID
DPRE@	DP re-driver function
NODPRE@	Disable DP re-driver
MIRROR@	For mirror function
ME@	ME Connector
EMC@	For EMC function
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
U31@	For U3 port1 redriver function
U32@	For U3 port2 redriver function
U33@	For U3 port3 redriver function
NU3R@	No U3 redriver function (All port)
RF@	For RF function
TS@	For Touch function

			RV104	RV105
Memory (GDDR3)				
Samsung	1G	SA22225SH30*4	PU 8.45K	PD 2K
	2G	SA000063F00*4	PU 3.4K	PD 10K
Hynix	1G	SA00005VS10*4	PU 4.53K	PD 2K
	2G	SA00005YL10*4	PU 4.75K	NC
Micron	1G	SA00005M100*4	NC	PD 4.75K
	2G	SA000060I00*4	PU 3.24K	PD 5.62K










The diagram illustrates two PCB layout techniques for SODIMM components:

- Side-By-Side placement:** Shows two SODIMM components (CH0 and CH1) placed side-by-side on the PCB. The SKL component is shown below them. The PCB is represented by a green bar at the bottom.
- Butterfly placement:** Shows two SODIMM components (CH0 and CH1) placed in a butterfly configuration on the PCB. The SKL component is shown below them. The PCB is represented by a green bar at the bottom.

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/05/07	Deciphered Date	2015/05/07	SKL(3/16):DDR3L CH.A	
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[23] DDR\_B\_D[0..63]  
[23] DDR\_B\_DQS#[0..7]  
[23] DDR\_B\_DQS[0..7]  
[23] DDR\_B\_MA[0..15]



UC1C

SKY\_UL1

©

DDR\_B\_D13 AF65  
DDR\_B\_D9 AF64  
DDR\_B\_D11 AK65  
DDR\_B\_D14 AK64  
DDR\_B\_D12 AF66  
DDR\_B\_D8 AF67  
DDR\_B\_D15 AK67  
DDR\_B\_D10 AK66  
DDR\_B\_D0 AF70  
DDR\_B\_D1 AF68  
DDR\_B\_D2 AH71  
DDR\_B\_D3 AH68  
DDR\_B\_D5 AF71  
DDR\_B\_D4 AF69  
DDR\_B\_D7 AH70  
DDR\_B\_D6 AH69  
DDR\_B\_D24 AT66  
DDR\_B\_D25 AU66  
DDR\_B\_D26 AP65  
DDR\_B\_D27 AN65  
DDR\_B\_D29 AN66  
DDR\_B\_D28 AP66  
DDR\_B\_D30 AT65  
DDR\_B\_D31 AU65  
DDR\_B\_D16 AT61  
DDR\_B\_D17 AU61  
DDR\_B\_D18 AP60  
DDR\_B\_D19 AN60  
DDR\_B\_D21 AN61  
DDR\_B\_D20 AP61  
DDR\_B\_D22 AT60  
DDR\_B\_D23 AU60  
DDR\_B\_D32 AU40  
DDR\_B\_D33 AT40  
DDR\_B\_D34 AT37  
DDR\_B\_D35 AU37  
DDR\_B\_D36 AR40  
DDR\_B\_D37 AP40  
DDR\_B\_D38 AP37  
DDR\_B\_D39 AR37  
DDR\_B\_D40 AT33  
DDR\_B\_D41 AU33  
DDR\_B\_D42 AU30  
DDR\_B\_D43 AT30  
DDR\_B\_D44 AR33  
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DDR\_B\_D46 AR30  
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DDR\_B\_D51 AP27  
DDR\_B\_D52 AN27  
DDR\_B\_D53 AN25  
DDR\_B\_D54 AP25  
DDR\_B\_D55 AT22  
DDR\_B\_D56 AU22  
DDR\_B\_D57 AU21  
DDR\_B\_D58 AT21  
DDR\_B\_D59 AN22  
DDR\_B\_D60 AP22  
DDR\_B\_D61 AN21  
DDR\_B\_D62 AN21  
DDR1\_DQ[63]

SKYLAKE-U\_BGA1356  
REV = 1

DDR CH - B

3 OF 20

DDR1\_CKIN[0]  
DDR1\_CKIN[1]  
DDR1\_CKP[0]  
DDR1\_CKP[1]  
DDR1\_CKE[0]  
DDR1\_CKE[1]  
DDR1\_CKE[2]  
DDR1\_CKE[3]  
DDR1\_CS[0]  
DDR1\_CS[1]  
DDR1\_ODT[0]  
DDR1\_ODT[1]  
DDR1\_MA[5]/DDR1\_CAA[0]/DDR1\_MA[5]  
DDR1\_MA[9]/DDR1\_CAA[1]/DDR1\_MA[9]  
DDR1\_MA[6]/DDR1\_CAA[2]/DDR1\_MA[6]  
DDR1\_MA[8]/DDR1\_CAA[3]/DDR1\_MA[8]  
DDR1\_MA[7]/DDR1\_CAA[4]/DDR1\_MA[7]  
DDR1\_MA[2]/DDR1\_CAA[5]/DDR1\_MA[2]  
DDR1\_MA[12]/DDR1\_CAA[6]/DDR1\_MA[12]  
DDR1\_MA[11]/DDR1\_CAA[7]/DDR1\_MA[11]  
DDR1\_MA[15]/DDR1\_CAA[8]/DDR1\_MA[15]  
DDR1\_MA[14]/DDR1\_CAA[9]/DDR1\_MA[14]  
DDR1\_MA[13]/DDR1\_CAB[0]/DDR1\_MA[13]  
DDR1\_CAS#/DDR1\_CAB[1]/DDR1\_MA[13]  
DDR1\_WE#/DDR1\_CAB[2]/DDR1\_MA[14]  
DDR1\_RAS#/DDR1\_CAB[3]/DDR1\_MA[16]  
DDR1\_BA[0]/DDR1\_CAB[4]/DDR1\_MA[16]  
DDR1\_MA[2]/DDR1\_CAB[5]/DDR1\_MA[2]  
DDR1\_BA[1]/DDR1\_CAB[6]/DDR1\_MA[1]  
DDR1\_MA[10]/DDR1\_CAB[7]/DDR1\_MA[10]  
DDR1\_MA[7]/DDR1\_CAB[8]/DDR1\_MA[1]  
DDR1\_MA[0]/DDR1\_CAB[9]/DDR1\_MA[0]  
DDR1\_MA[9]  
DDR1\_MA[3]  
DDR1\_DQS[0]/DDR1\_DQS[2]  
DDR1\_DQS[0]/DDR1\_DQS[2]  
DDR1\_DQS[1]/DDR1\_DQS[3]  
DDR1\_DQS[4]/DDR1\_DQS[6]  
DDR1\_DQS[2]/DDR1\_DQS[6]  
DDR1\_DQS[3]/DDR1\_DQS[7]  
DDR1\_DQS[4]/DDR1\_DQS[2]  
DDR1\_DQS[4]/DDR1\_DQS[2]  
DDR1\_DQS[4]/DDR1\_DQS[2]  
DDR1\_DQS[5]/DDR1\_DQS[3]  
DDR1\_DQS[5]/DDR1\_DQS[3]  
DDR1\_DQS[6]  
DDR1\_DQS[7]  
DDR1\_DQS[7]  
DDR1\_ALERT#  
DDR1\_ALERT#  
DDR1\_PAR  
DRAM\_RESET#  
DDR\_RCOMP[0]  
DDR\_RCOMP[1]  
DDR\_RCOMP[2]

AN45 SB\_CLK\_DDR#0  
AN46 SB\_CLK\_DDR#1  
AP45 SB\_CLK\_DDR0  
AP46 SB\_CLK\_DDR1  
AN56 DDRB\_CKE0\_DIMMB#  
AP55 DDRB\_CKE1\_DIMMB#  
AN55 DIMMB#  
AP53 X  
BB42 DDRB\_CS0\_DIMMB#  
BA42 DDRB\_CS1\_DIMMB#  
AW42 DDRB\_ODT0\_DIMMB#  
AY48 DDRB\_MA5  
AP50 DDRB\_MA9  
BA49 DDRB\_MA6  
BB48 DDRB\_MA8  
AP48 DDRB\_MA7  
AP51 DDRB\_MA2  
AN50 DDRB\_MA12  
AN48 DDRB\_MA11  
AN52 DDRB\_MA15  
AN52 DDRB\_MA14  
BA43 DDRB\_MA13  
AY43 DDRB\_CAS#  
AY44 DDRB\_RAS#  
AW44 DDRB\_BS0  
BB44 DDRB\_BS1  
AY47 DDRB\_BS2  
BA43 DDRB\_BS1  
AW46 DDRB\_MA10  
AY46 DDRB\_MA1  
BA46 DDRB\_MA3  
BA45 DDRB\_MA4  
BA47  
AH66 DDR\_B\_DQS#1  
AH65 DDR\_B\_DQS1  
AG69 DDR\_B\_DQS#0  
AG70 DDR\_B\_DQS0  
AR66 DDR\_B\_DQS#3  
AR65 DDR\_B\_DQS3  
AR61 DDR\_B\_DQS#2  
AR60 DDR\_B\_DQS2  
AT38 DDR\_B\_DQS#4  
AR38 DDR\_B\_DQS#4  
AT32 DDR\_B\_DQS#5  
AR32 DDR\_B\_DQS5  
AR25 DDR\_B\_DQS#6  
AR27 DDR\_B\_DQS6  
AR22 DDR\_B\_DQS#7  
AR21 DDR\_B\_DQS7  
AN43 DDR1\_ALERT#  
AT19 DDR3\_DRAMRST#  
AT18 SM\_RCOMP0  
AT18 SM\_RCOMP1  
AT18 SM\_RCOMP2  
RC8 1 2 121 0402 1%  
RC9 1 2 80.6 0402 1%  
RC10 1 2 100 0402 1%

20141202

20141022

[SKL PDG]for DDR3L  
DDR\_RCOMP[0] Pull down 121 ohm resistor  
DDR\_RCOMP[1] Pull down 80.6 ohm resistor  
DDR\_RCOMP[2] Pull down 100 ohm resistor

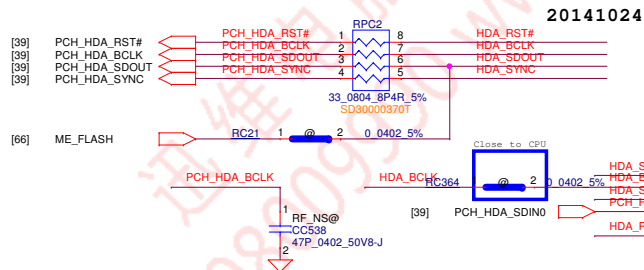
[SKL PDG]DDR\_RCOMP  
1. Trace width=12~15 mils, Spacing=20mil, Max length=500mils  
2. R close to MCP

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Title				LCFC	
SKL(4/16):DDR3L CH.B					
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[SKL PDG] Manufacturing Mode Jumper

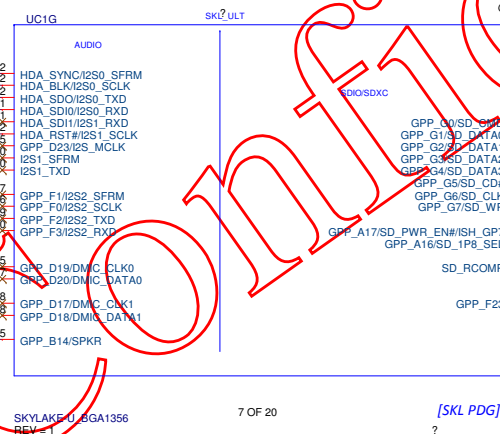
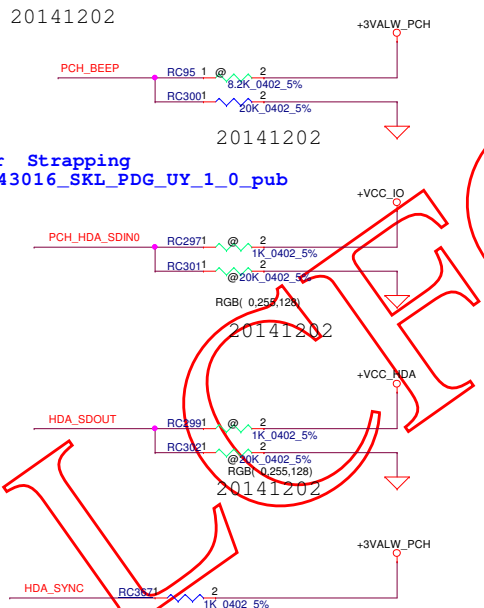
1. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default)
2. If sampled high, the Flash Descriptor Security will be overridden.



GPP\_B14, Internal PD 20K  
No Reboot on TCO  
Timer expiration  
pull-up to VCC3\_3 through a 1- 8.2 KΩ ± %  
resistor to disable this capability

20141202

Processor Strapping  
543016\_543016\_SKL\_PDG\_UY\_1\_0\_pub  
P780

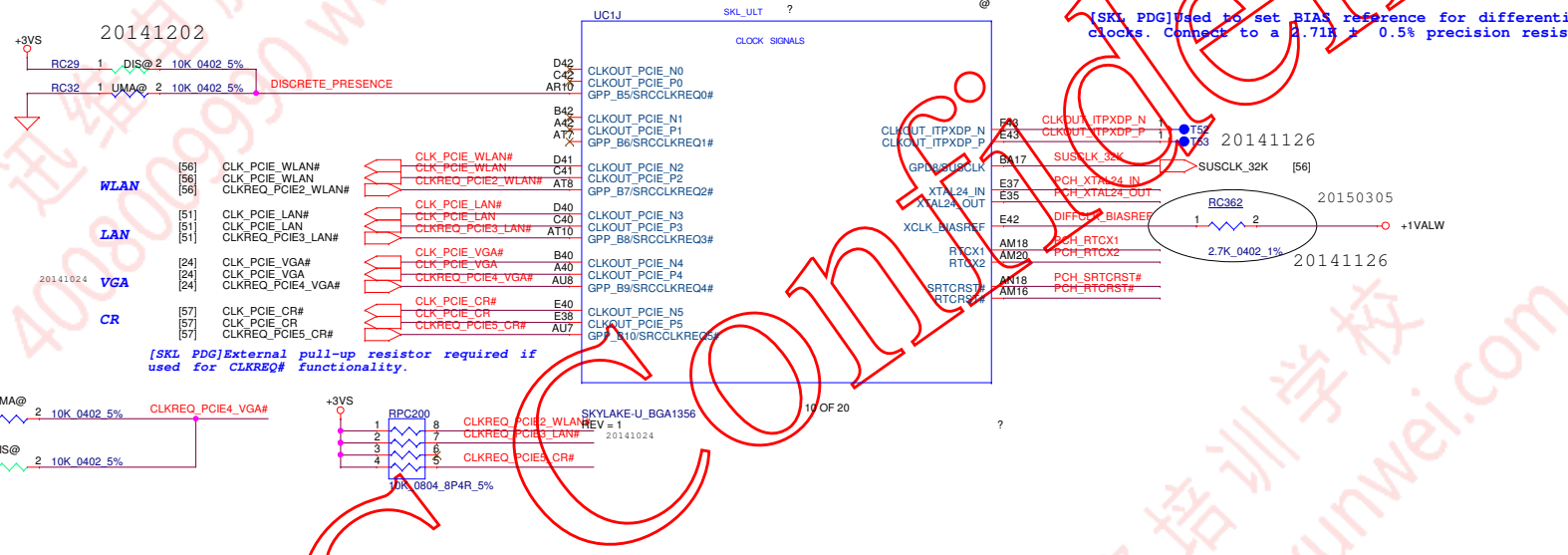


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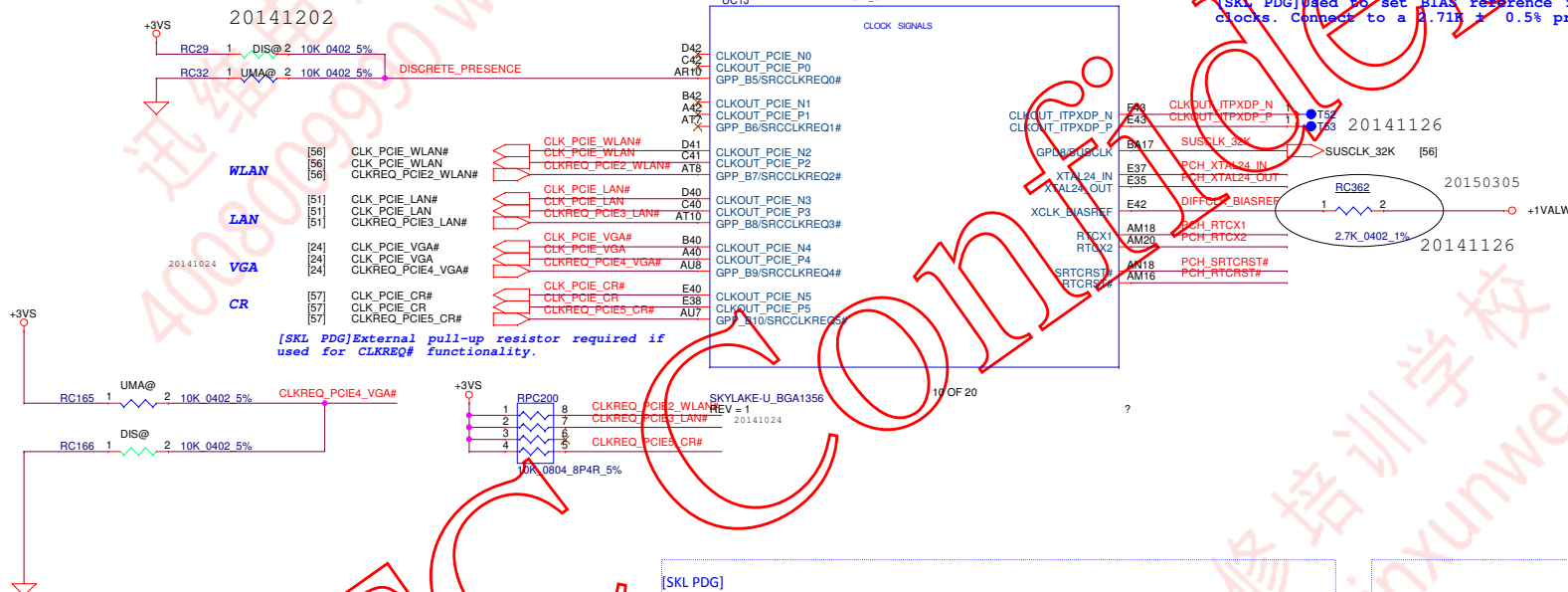
Title		SKL(5/16):HDA/SDIO	
Size	Document Number	Rev	1.0
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JCMOS, JME Setting, Need Under DDR Door



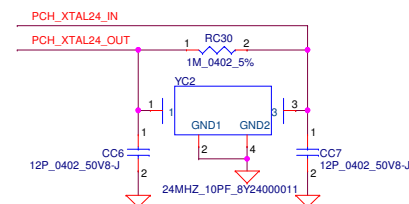
[SKL PDG] External pull-up resistor required if used for CLKREQ# functionality.




[SKL PDG]  
1.Space > 15mils  
2.No trace under crystal  
3.Place on opposit side of MCP for temp inf l uence  
4.The exact capacitor values forC1 and C2 must be based on the crystal maker recommendat i ons  
Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.

[SKL PDG]Max Crystal ESR = 50k Ohm

[SKL PDG]  
1.A 24 MHz crystal with crystal frequency tolerance and stability of +/-30 ppm  
2.Two External Load Capacitors (Ce1 and Ce2)  
3.A 1-Mohm bias resistor (Rf)

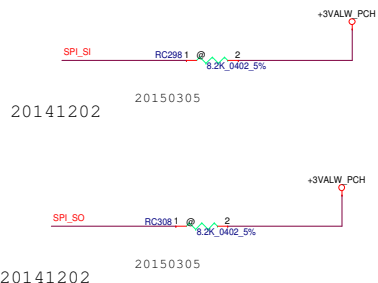


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Issued Date	2014/05/07	Deciphered Date	2015/05/07	SKL(6/16):CLOCK SIGNALS	
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# Functional Strap Definitions

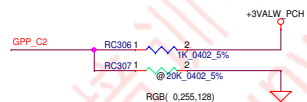
## SPI0\_MOSI

This signal has an internal pull-up.  
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



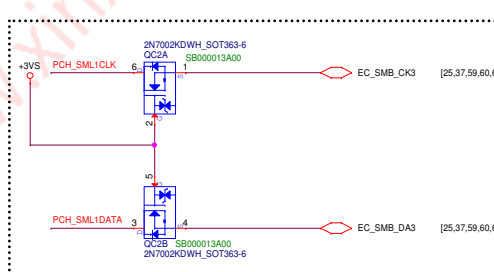
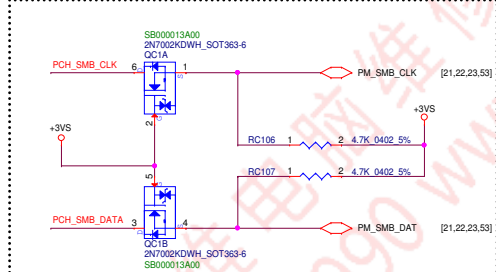
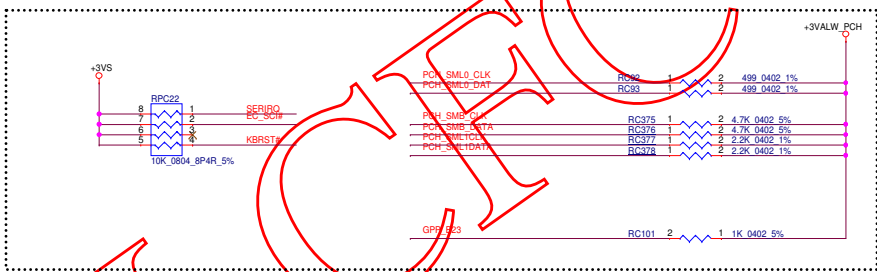
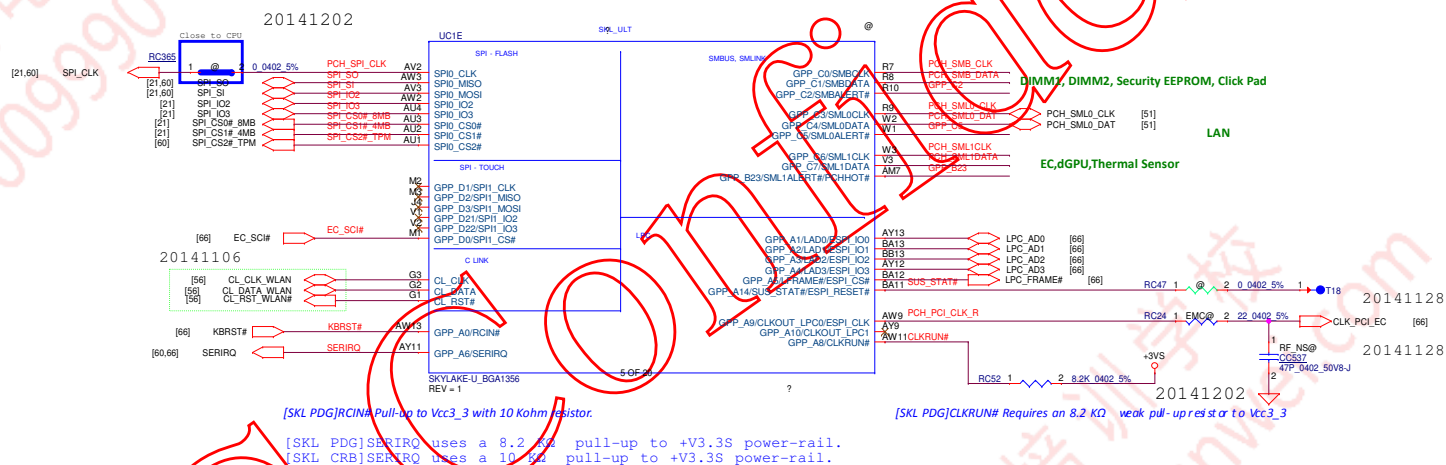
## GPP\_C2, Internal PD 20K

L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).  
\*H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).Support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



## GPP\_C5, Internal PD 20K

\*L: LPC  
H: eSPI

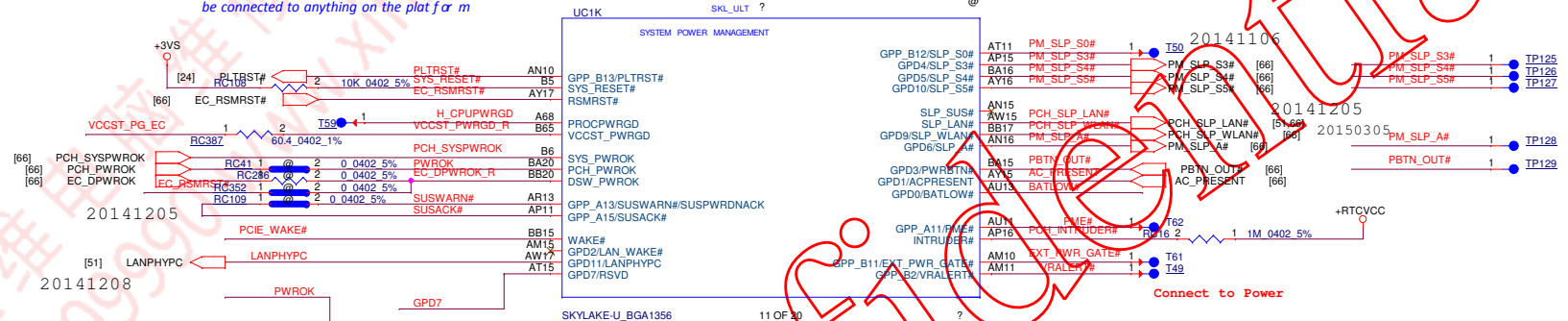


[SKL PDG]SYS\_RESET#: Connect this signal on PCH directly to the reset but t on and pull-up its g nd to +V3.3V c a e r a l t h r o u g h a weak pull-up resistor (8.2~10 Kohm).

[SKL PDG]PROCPWRGD  
1. Indicates that VCCIN, VDDQ power supplies and clocks are stable. This signal will be asserted only after PCH\_PWRCK assertion.  
2. PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the platform.

[SKL PDG]SLP\_S3, SLP\_S4, SLP\_S5 No pull-up/pull-down resistors needed. Signals driven by the PCH.

[SKL PDG]SLP\_A: No pull-up/pull-down resistors needed. Signals driven by the PCH. Can be left as NC when the Intel Management Engine (Intel ME) is not supported on the platform. When asserted (driven low) it is not supported on the platform.



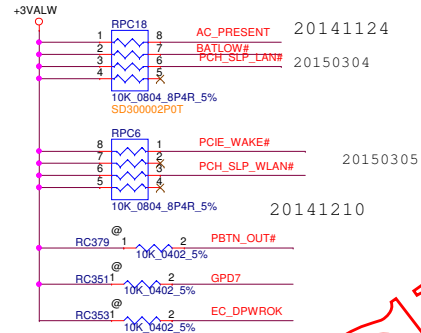
[SKL PDG]AC\_PRESENT: 8.2~10 K $\Omega$  pull-up to DS Wvl.

[SKL PDG]BATLOW#: 8.2~10 K $\Omega$  pull-up to DS Wvl.

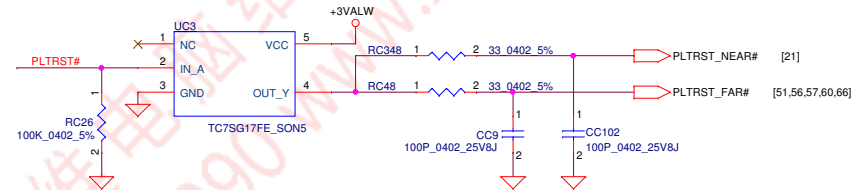
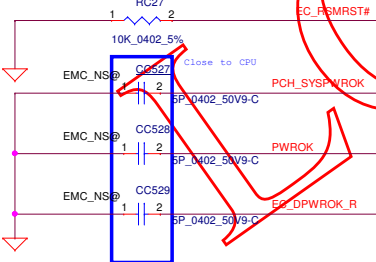
[SKL PDG]WAKE#: 10 K $\Omega$  pull-up to Vcc DS V3\_3

[SKL PDG]APWROK: There is no corresponding APWROK signal input to the PCH, but the PCH does have an internally generated version of APWROK that is tied to mSLP\_A#.

[SKL PDG]EXT\_PWR\_GATE# (External Power Gate)  
1. HSIO Power Control: Used to control power to VCCMPHYGT\_1p0, VCCMPHYPLL\_1p0 and VCCSRAM\_1p0 in S0 & Sx.  
2. PCH will drive EXT\_PWR\_GATE# low when all the high speed IO controllers (xHCI, SATA and PCIe) are idle or have no devices attached.



[SKL PDG]RSMRST#: Recommend an 8.2~10 Kohm pull-down resistor to ground.  
Note: CRB uses 10 K $\Omega$  pull-down

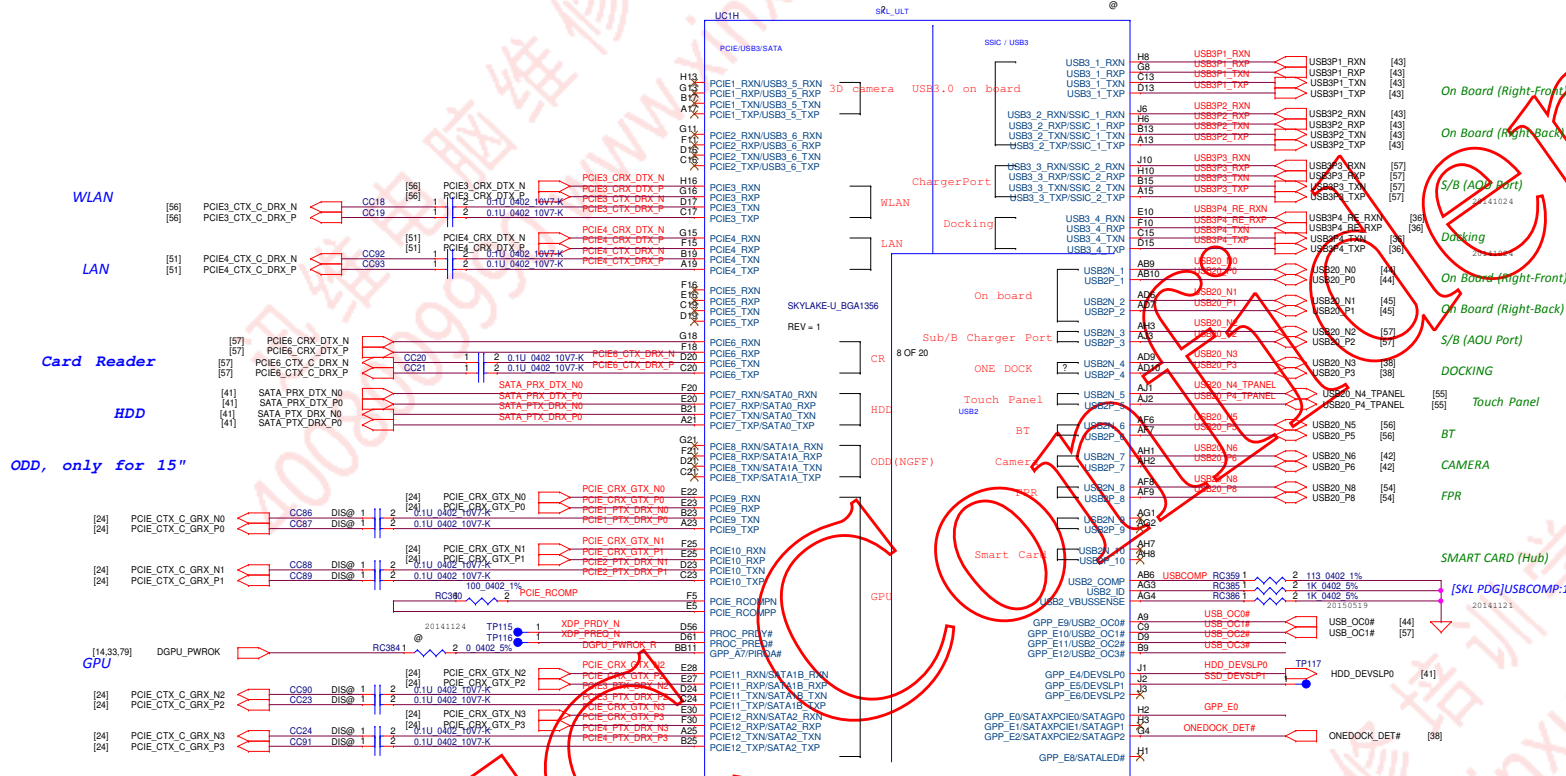


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		2015/05/07		SKL(8/16):SYSTEM PM	
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Size		Document Number		Rev	
Custom		BE460 NW-A551		1.0	
Date:		Wednesday, August 05, 2015		Sheet 12 of 83	







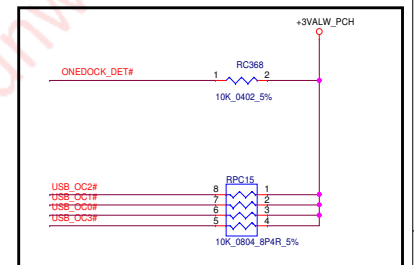


[SKL PDG]PCIE\_RCOMP  
1.100 ohm +/-0.1% external resistor between RCOMP/RCOMP\_N

2.SATA compensation circuit is code share with  
PCIE\_RCOMP/N differential pair. Refer to RD Express  
Design Guidelines chapter for PCIE\_RCOMP/N guideline.

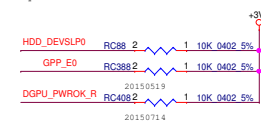
3.Width:12~15Mil  
Space:~12Mil  
Length:Both RCOMP & RCOMP\_N need to matched to less than 1% trace and board

USB Port Number	USB Port Number
USB_OC0#	Port 0, Port1
USB_OC1#	Port 2, Port3
USB_OC2#	Port 4, Port5
USB_OC3#	Port 6, Port7

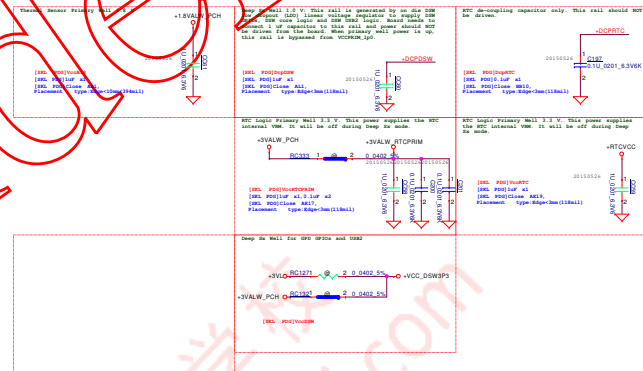



[SKL PDG] OC [x] pins require a pull-up to VccSus3\_3 with 8.2~10 Kohm resistors

[SKL PCH EDS]no external pull-up or pull-down termination  
required when used as DEVSLP








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Size	Document Number	<p><b>B2480-NW-A551</b></p>	

GND 1 OF 3		
A5	VSS_A5	VSS_AL65
A67	VSS_A67	VSS_AL66
A70	VSS_A70	VSS_AM13
AA2	VSS_AA2	VSS_AM21
AA4	VSS_AA4	VSS_AM25
AA65	VSS_AA65	VSS_AM27
AA68	VSS_AA68	VSS_AM43
AB15	VSS_AB15	VSS_AM44
AB16	VSS_AB16	VSS_AM45
AB18	VSS_AB18	VSS_AM46
AB21	VSS_AB21	VSS_AM55
AB22	VSS_AB22	VSS_AM60
AB8	VSS_AB8	VSS_AM61
AD13	VSS_AD13	VSS_AM68
AD16	VSS_AD16	VSS_AM71
AD19	VSS_AD19	VSS_AM8
AD20	VSS_AD20	VSS_AM8
AD21	VSS_AD21	VSS_AN20
AD22	VSS_AD22	VSS_AN23
AD8	VSS_AD8	VSS_AN28
AE64	VSS_AE64	VSS_AN30
AE65	VSS_AE65	VSS_AN32
AE66	VSS_AE66	VSS_AN33
AE67	VSS_AE67	VSS_AN35
AE68	VSS_AE68	VSS_AN37
AE69	VSS_AE69	VSS_AN38
AF1	VSS_AF1	VSS_AN40
AF10	VSS_AF10	VSS_AN42
AF15	VSS_AF15	VSS_AN43
AF17	VSS_AF17	VSS_AN44
AF2	VSS_AF2	VSS_AN48
AF4	VSS_AF4	VSS_AP10
AF63	VSS_AF63	VSS_AP18
AG16	VSS_AG16	VSS_AP20
AG17	VSS_AG17	VSS_AP23
AG18	VSS_AG18	VSS_AP28
AG19	VSS_AG19	VSS_AP32
AG20	VSS_AG20	VSS_AP35
AG21	VSS_AG21	VSS_AP38
AG71	VSS_AG71	VSS_AP42
AH13	VSS_AH13	VSS_AP58
AH6	VSS_AH6	VSS_AP63
AH63	VSS_AH63	VSS_AP68
AH64	VSS_AH64	VSS_AP70
AH67	VSS_AH67	VSS_AR11
AJ15	VSS_AJ15	VSS_AR15
AJ18	VSS_AJ18	VSS_AR16
AJ20	VSS_AJ20	VSS_AR20
AJ4	VSS_AJ4	VSS_AR23
AK11	VSS_AK11	VSS_AR28
AK16	VSS_AK16	VSS_AR35
AK18	VSS_AK18	VSS_AR42
AK21	VSS_AK21	VSS_AR43
AK22	VSS_AK22	VSS_AR44
AK27	VSS_AK27	VSS_AR48
AK63	VSS_AK63	VSS_AR5
AK68	VSS_AK68	VSS_AR50
AK69	VSS_AK69	VSS_AR52
AK8	VSS_AK8	VSS_AR53
AL2	VSS_AL2	VSS_AR58
AL28	VSS_AL28	VSS_AR63
AL32	VSS_AL32	VSS_AR8
AL35	VSS_AL35	VSS_AT2
AL38	VSS_AL38	VSS_AT20
AL4	VSS_AL4	VSS_AT23
AL45	VSS_AL45	VSS_AT28
AL48	VSS_AL48	VSS_AT35
AL52	VSS_AL52	VSS_AT44
AL55	VSS_AL55	VSS_AT56
AL58	VSS_AL58	VSS_AT58
AL64	VSS_AL64	VSS_AT95

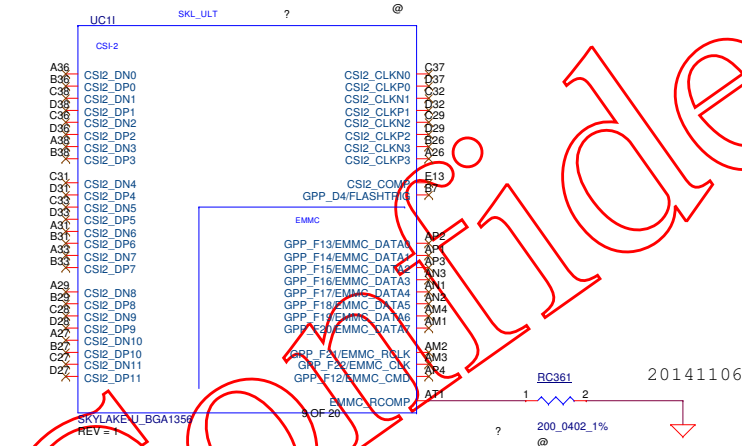
GND 2 OF 3		
AT63	VSS_AT63	VSS_BA49
AT68	VSS_AT68	VSS_BA53
AT71	VSS_AT71	VSS_BA57
AU10	VSS_AU10	VSS_BA6
AU15	VSS_AU15	VSS_BA62
AU20	VSS_AU20	VSS_BA66
AU32	VSS_AU32	VSS_BA66
AU38	VSS_AU38	VSS_BA71
AV1	VSS_AV1	VSS_BB18
AV68	VSS_AV68	VSS_BB26
AV69	VSS_AV69	VSS_BB30
AV70	VSS_AV70	VSS_BB34
AV71	VSS_AV71	VSS_BB38
AW10	VSS_AW10	VSS_BB43
AW12	VSS_AW12	VSS_BB43
AW14	VSS_AW14	VSS_BB43
AW16	VSS_AW16	VSS_BB43
AW18	VSS_AW18	VSS_BB43
AW21	VSS_AW21	VSS_BB43
AW23	VSS_AW23	VSS_BB43
AW26	VSS_AW26	VSS_BB43
AW28	VSS_AW28	VSS_BB43
AW30	VSS_AW30	VSS_BB43
AW32	VSS_AW32	VSS_BB43
AW34	VSS_AW34	VSS_BB43
AW36	VSS_AW36	VSS_BB43
AW38	VSS_AW38	VSS_BB43
AW41	VSS_AW41	VSS_BB43
AW43	VSS_AW43	VSS_BB43
AW45	VSS_AW45	VSS_BB43
AW47	VSS_AW47	VSS_BB43
AW49	VSS_AW49	VSS_BB43
AW51	VSS_AW51	VSS_BB43
AW53	VSS_AW53	VSS_BB43
AW55	VSS_AW55	VSS_BB43
AW57	VSS_AW57	VSS_BB43
AW6	VSS_AW6	VSS_BB43
AW60	VSS_AW60	VSS_BB43
AW62	VSS_AW62	VSS_BB43
AW64	VSS_AW64	VSS_BB43
AW66	VSS_AW66	VSS_BB43
AW68	VSS_AW68	VSS_BB43
AW8	VSS_AW8	VSS_BB43
AY66	VSS_AY66	VSS_BB43
B10	VSS_B10	VSS_BB43
B14	VSS_B14	VSS_BB43
B18	VSS_B18	VSS_BB43
B22	VSS_B22	VSS_BB43
B30	VSS_B30	VSS_BB43
B34	VSS_B34	VSS_BB43
B39	VSS_B39	VSS_BB43
B41	VSS_B41	VSS_BB43
B43	VSS_B43	VSS_BB43
B45	VSS_B45	VSS_BB43
B47	VSS_B47	VSS_BB43
B49	VSS_B49	VSS_BB43
B53	VSS_B53	VSS_BB43
B58	VSS_B58	VSS_BB43
B62	VSS_B62	VSS_BB43
B66	VSS_B66	VSS_BB43
B71	VSS_B71	VSS_BB43
BA1	VSS_BA1	VSS_BB43
BA10	VSS_BA10	VSS_BB43
BA14	VSS_BA14	VSS_BB43
BA18	VSS_BA18	VSS_BB43
BA2	VSS_BA2	VSS_BB43
BA23	VSS_BA23	VSS_BB43
BA28	VSS_BA28	VSS_BB43
BA32	VSS_BA32	VSS_BB43
BA36	VSS_BA36	VSS_BB43
F68	VSS_F68	VSS_BB43
BA45	VSS_BA45	VSS_BB43
VSS_BA45		VSS_BB43


GND 3 OF 3		
F8	VSS_F8	VSS_L18
G10	VSS_G10	VSS_L2
G22	VSS_G22	VSS_L20
G43	VSS_G43	VSS_L4
G45	VSS_G45	VSS_L8
G48	VSS_G48	VSS_L8
G5	VSS_G5	VSS_N10
G52	VSS_G52	VSS_N13
G55	VSS_G55	VSS_N19
G58	VSS_G58	VSS_N21
G6	VSS_G6	VSS_N21
G66	VSS_G66	VSS_N21
H15	VSS_H15	VSS_N21
H18	VSS_H18	VSS_N21
H71	VSS_H71	VSS_N21
J13	VSS_J13	VSS_N21
J25	VSS_J25	VSS_N21
J28	VSS_J28	VSS_N21
J32	VSS_J32	VSS_N21
J35	VSS_J35	VSS_N21
J38	VSS_J38	VSS_N21
J42	VSS_J42	VSS_N21
K16	VSS_K16	VSS_N21
K18	VSS_K18	VSS_N21
K22	VSS_K22	VSS_N21
K61	VSS_K61	VSS_N21
K63	VSS_K63	VSS_N21
K64	VSS_K64	VSS_N21
K65	VSS_K65	VSS_N21
K66	VSS_K66	VSS_N21
K67	VSS_K67	VSS_N21
K71	VSS_K71	VSS_N21
L11	VSS_L11	VSS_N21
L16	VSS_L16	VSS_N21
L17	VSS_L17	VSS_N21

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Date:		Wednesday, August 05, 2015		Sheet		18 of 83	



LCFC

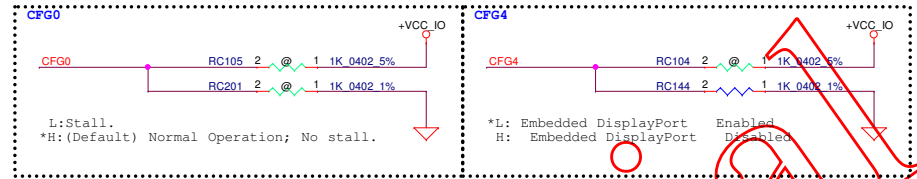


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				Custom	BE460 NW-A551		
				Date:	Wednesday, August 05, 2015	Sheet	19 of 83



20150309  
(Test point change to 12mil)

[SKL EDS]



TABLE

**CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted**  
1 : No Stall  
0 : Stall

**CFG4 : eDP Enable**  
1 : Disabled  
0 : Enabled

**CFG9 : SVID Bus Communication**  
1 : Enabled  
0 : Disabled

[SKL EDS]Zero Voltage Mode:VCCOPC is fixed OPC VR output voltage of 1V, the processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal as shown below:

ZVM#	state	VCCOPC
0V		0V
1V		1V

20141202

[SKL EDS]Minimum Speed Mode: VCCEPIO can be connected to OPC VR in this case VCCEPIO is fixed to 1V. The processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal. In order to achieve better power/performance it is recommended to use a separate VR for VCCEPIO in this case VCCEPIO is configurable to 0.8V/1V. The processor drives the VR to set VCCEPIO value(0.8V/1V) using MSM# signal, based on the required bandwidth for the EPIO interface as shown below:

ZVM#	state	MSM#	state	VCCEPIO
0V		X		0V
1V		0V		0.8V
1V		1V		1V

[SKL CRB]

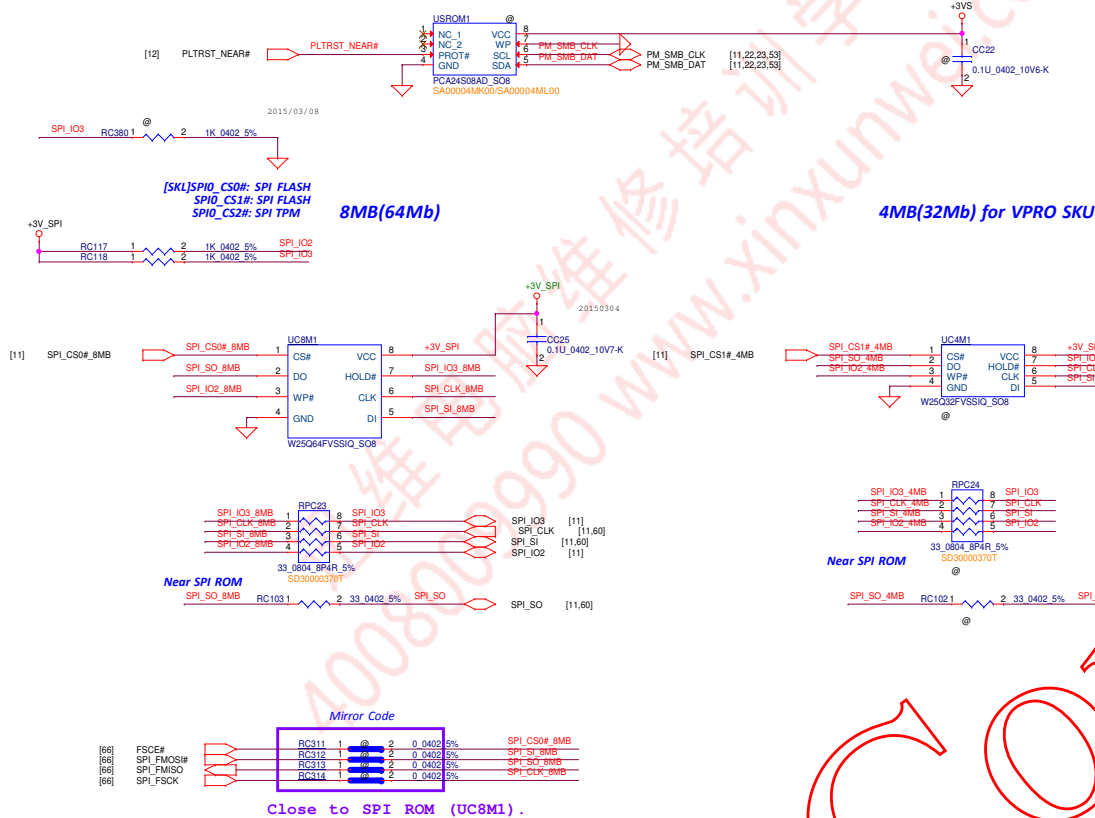
+1VALW\_PCH RC152 2 1 49.9 0402 1%  
RC354 2 1 1.5K 0402 5%  
[SKL PDG]Route HOOK[6] to Skylake ITP\_PMODE.  
Termination: Resistor value from 1K ohm to 3K ohm pull up to PCH\_V1.0A Rail.

[SKL CRB]

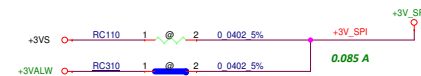
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Issued Date	2014/05/07	Deciphered Date	2015/05/07
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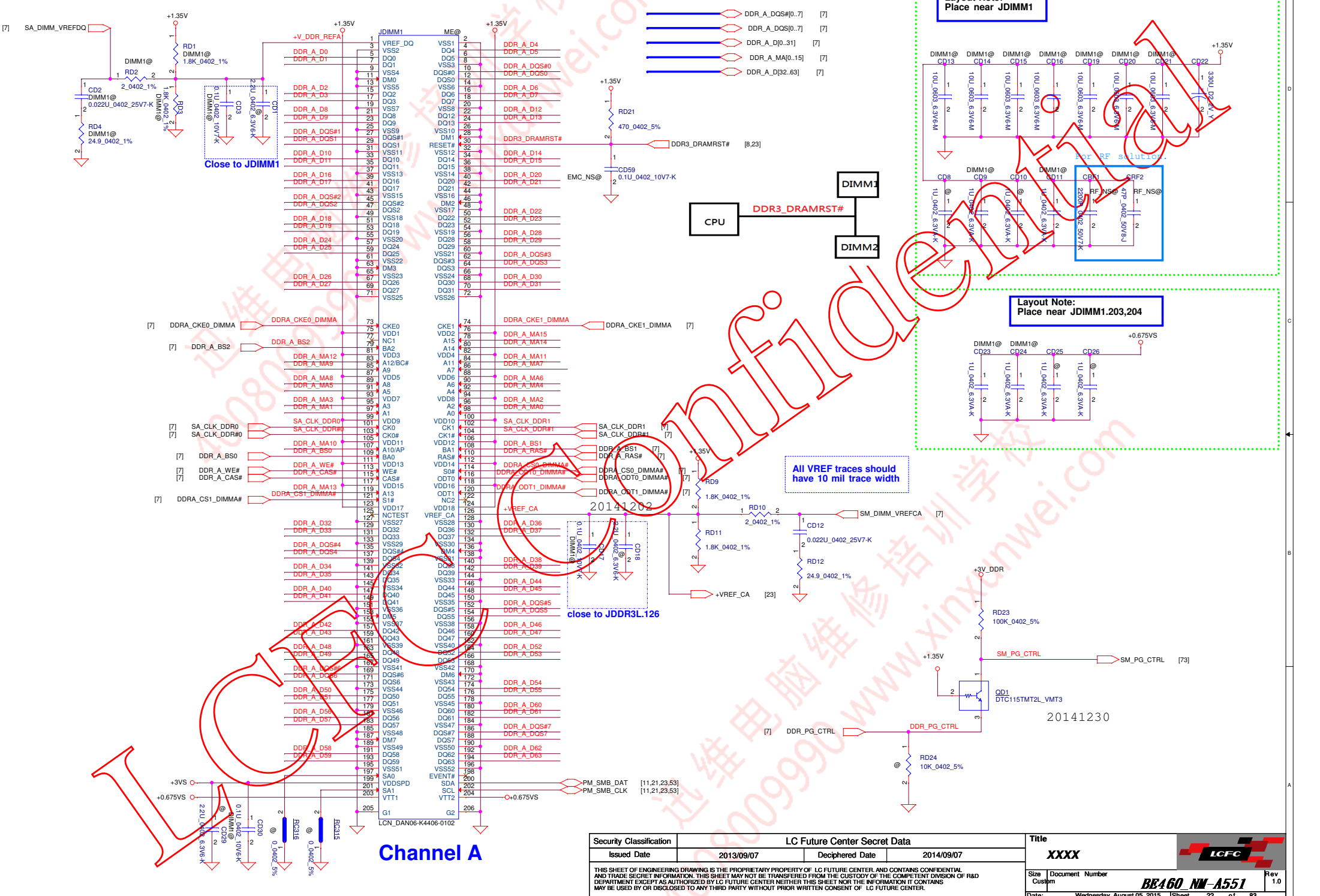
Size		Document Number		Rev	
Custom		BB460-NW-A551		1.0	
Date:		Wednesday, August 05, 2015		Sheet 20 of 83	

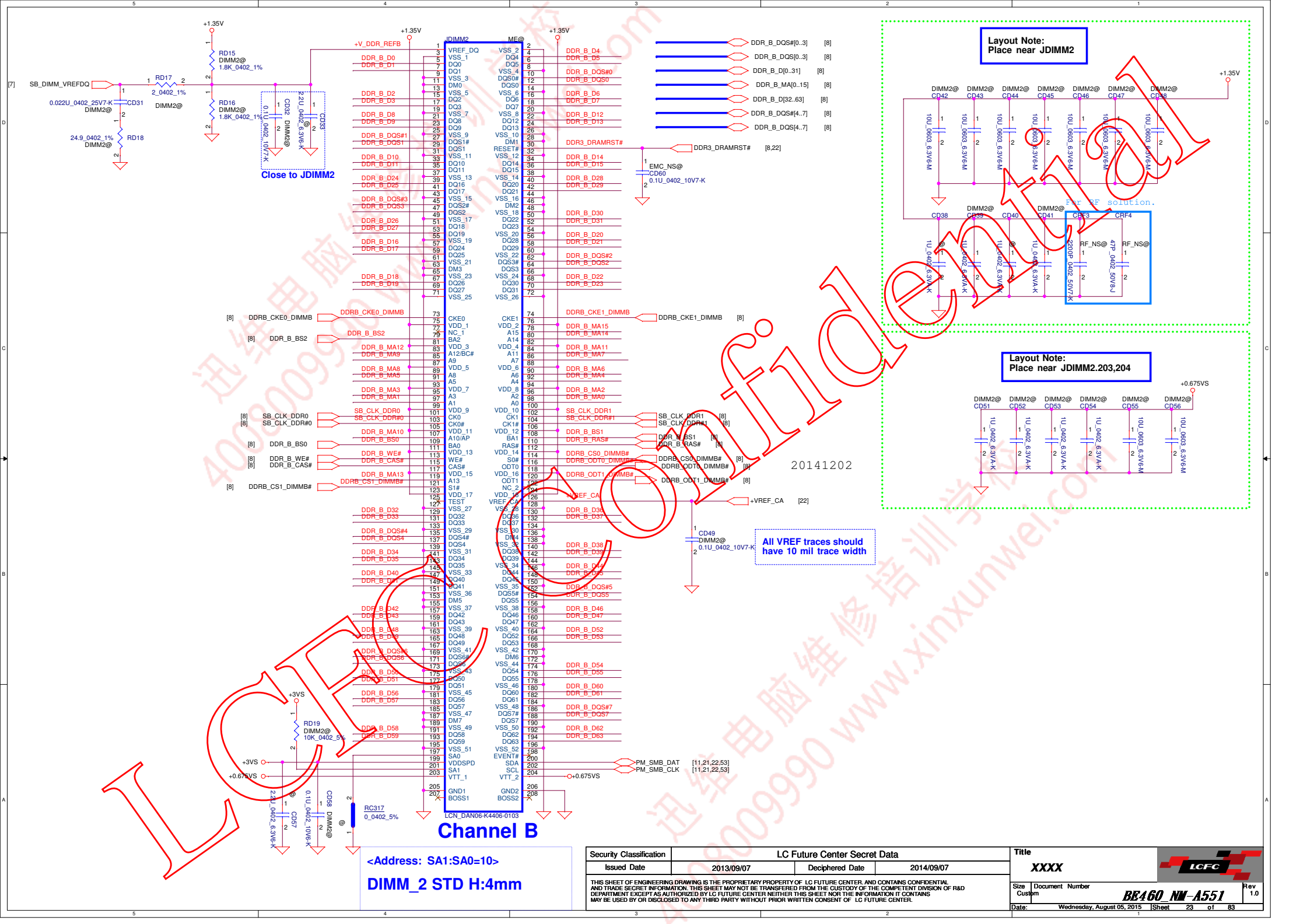
### Security ROM



## M3 Support + Intel LAN PHY / Wireless LAN Solution

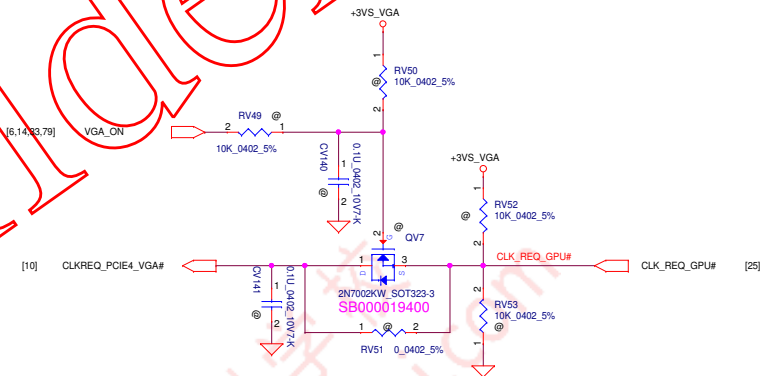
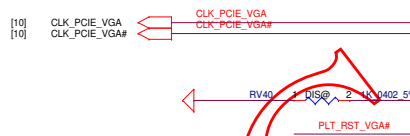
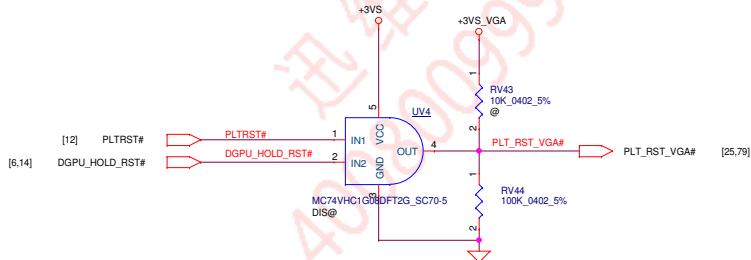
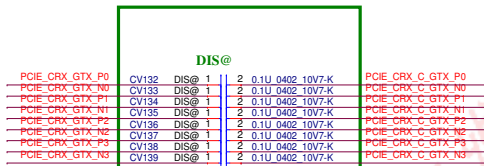




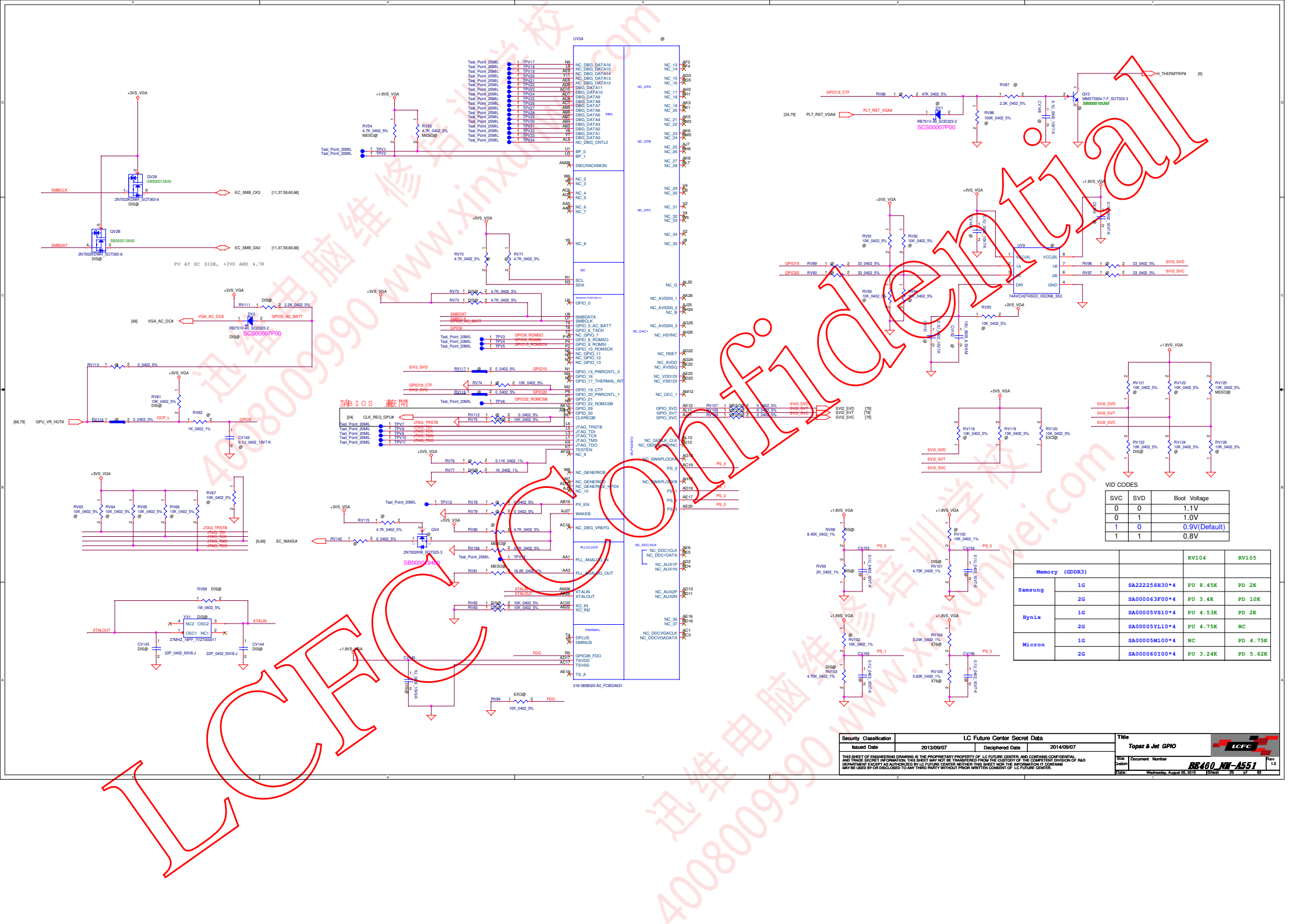




[15] PCIE\_CTX\_C\_GRX\_N[0..3] PCIE\_CTX\_C\_GRX\_N0..3  
[15] PCIE\_CTX\_C\_GRX\_P[0..3] PCIE\_CTX\_C\_GRX\_P0..3  
[15] PCIE\_CRX\_GTX\_N[0..3] PCIE\_CRX\_GTX\_N0..3  
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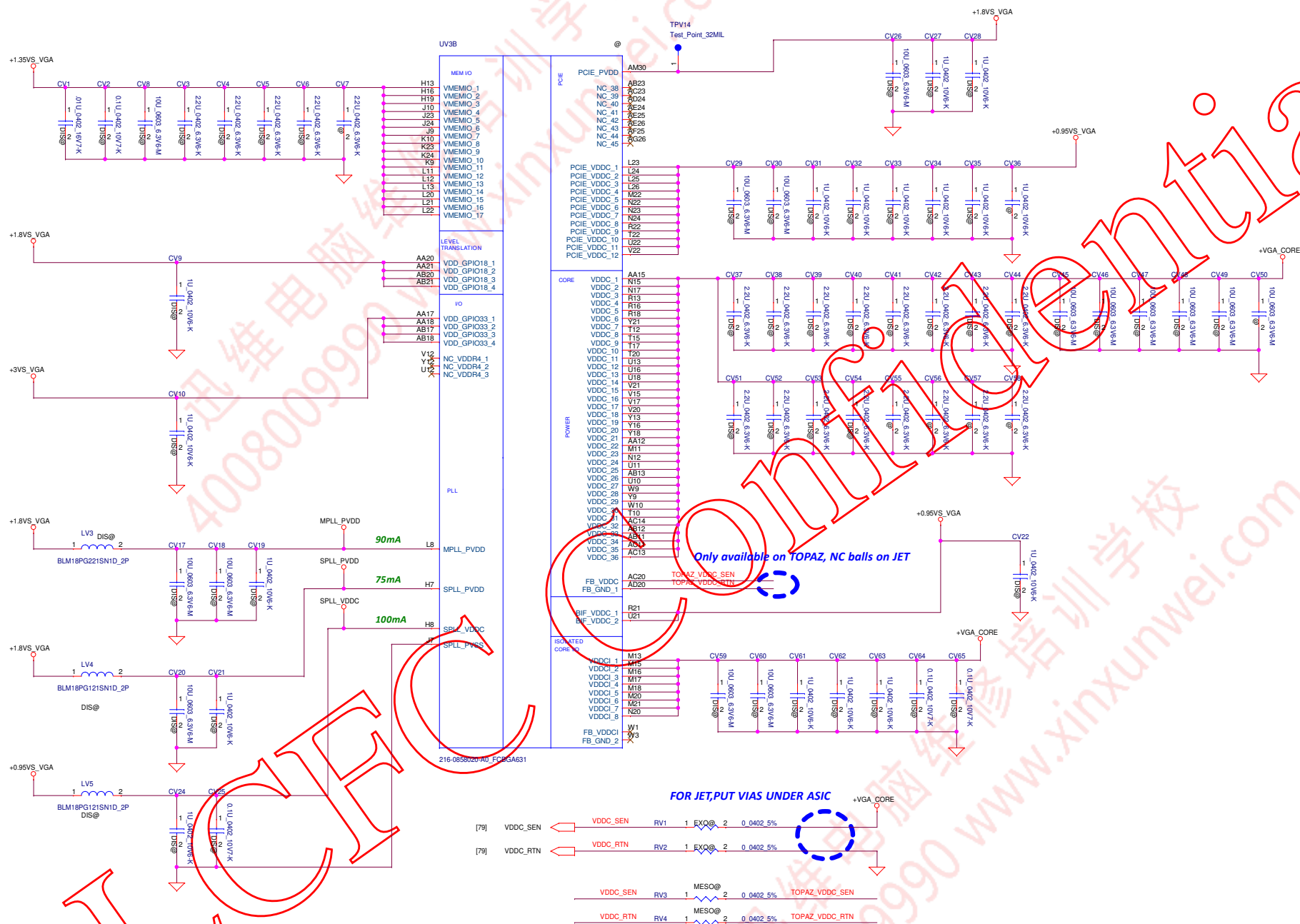


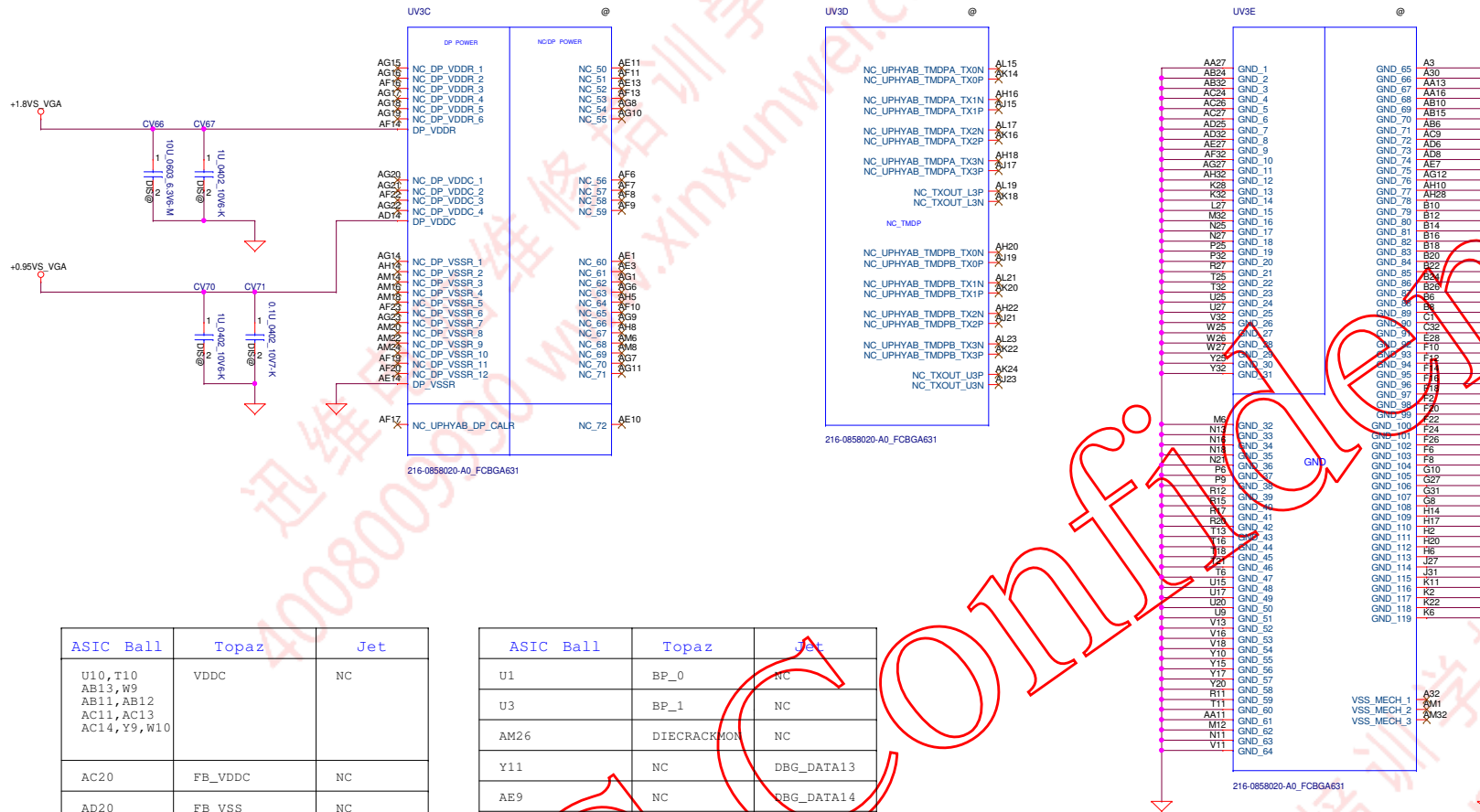
VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V

Memory (GDDR3)			RV104	RV105
Samsung	1G	SA222258H30*4	PU 8.45K	PD 2K
	2G	SA000063P00*4	PU 3.4K	PD 10K
Hynix	1G	SA00005V810*4	PU 4.53K	PD 2K
	2G	SA00005Y110*4	PU 4.75K	NC
Micron	1G	SA00005M100*4	NC	PD 4.75K
	2G	SA000060100*4	PU 3.24K	PD 5.62K

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/09/07	Deciphered Date	2014/09/07	Topaz & Jet GPIO	
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Rev	Document Number	Rev			
0100	0100	0100			
Wednesday, August 06, 2014 10:00					





ASIC Ball	Topaz	Jet
U10, T10 AB13, W9 AB11, AB12 AC11, AC13 AC14, Y9, W10	VDDC	NC
AC20	FB_VDDC	NC
AD20	FB_VSS	NC
W1	FB_VDDCI	NC
W3	FB_VSS	NC
AJ11	GPIO_SVC	NC_SVI2
AK12	GPIO_SVD	NC_SVI2
AL11	GPIO_SVT	NC_SVI2
N6	GPIO_11	NC_GPIO11
N5	GPIO_12	NC_GPIO12
N3	GPIO_13	NC_GPIO13
AJ27	WAKEB	NC_VSYNC
T8	PCC/GPIO_6	GPIO_6
AA	PLL_ANALOG_OUT	NC
AA1	PLL_ANALOG_IN	NC

ASIC Ball	Topaz	Jet
U1	BP_0	NC
U3	BP_1	NC
AM26	DIECRACKMON	NC
Y11	NC	DBG_DATA13
AE9	NC	DBG_DATA14
L9	NC	DBG_DATA15
N9	NC	DBG_DATA16
AE8	NC	DBG_DATA12
AL9	NC	DBG_CNTL0
H13, H15, H19, K10 J23, L24, M9, K10 K23, K24, K9, L11 L12, L13, L20, L21 L22	VDDMIO	VDDR1
AA17, AA18 AB17, AB18	VDD_GPIO33	VDDR3
AA20, AA21 AB20, AB21	VDD_GPIO18	VDD_CT

	Bits5	Bits4	Bits3	Bits2	Bits1
PS0	1	1	0	0	1
PS1	1	1	0	0	0
PS2	0	0	0	0	0
PS3	1	1	?	?	?

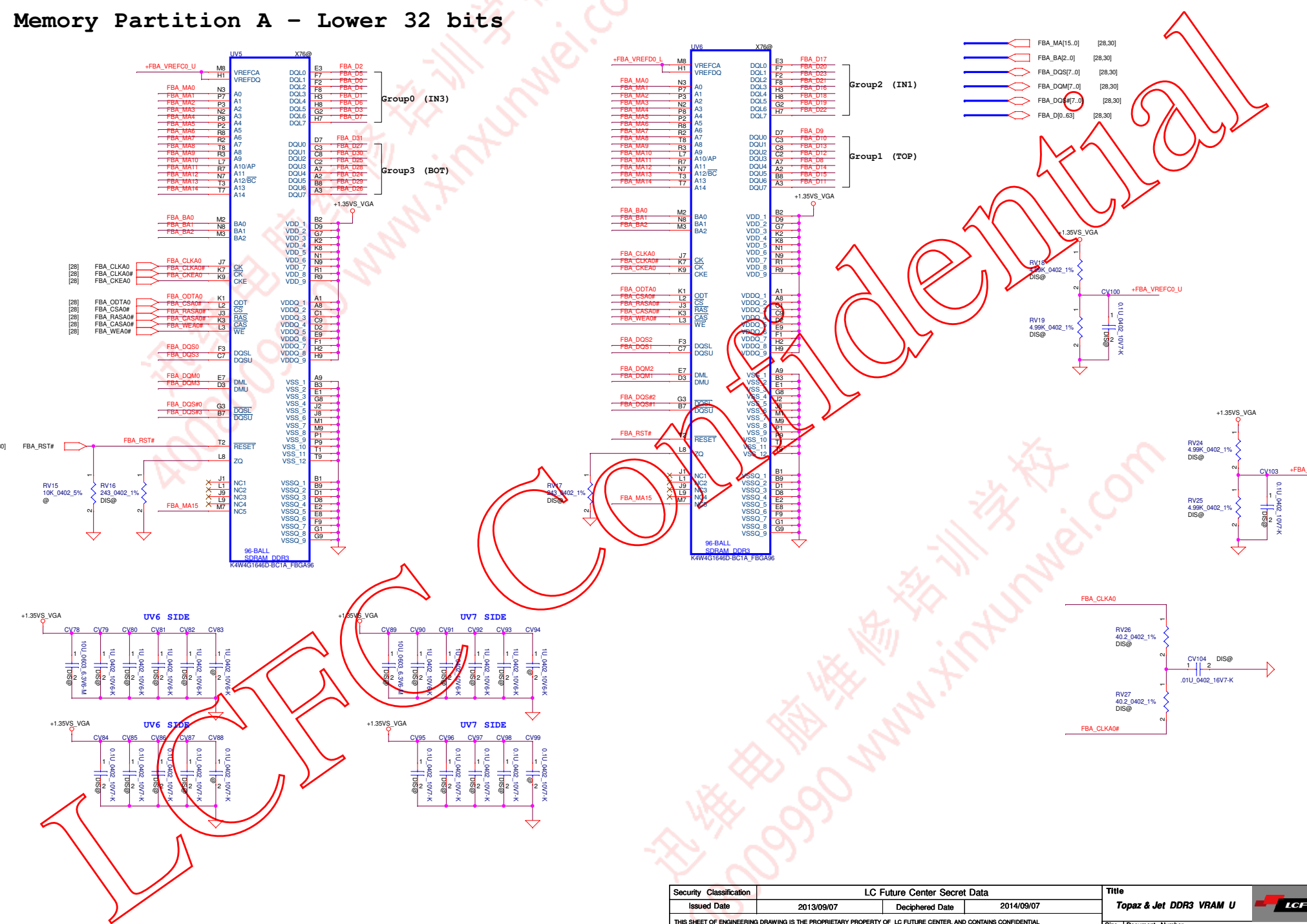
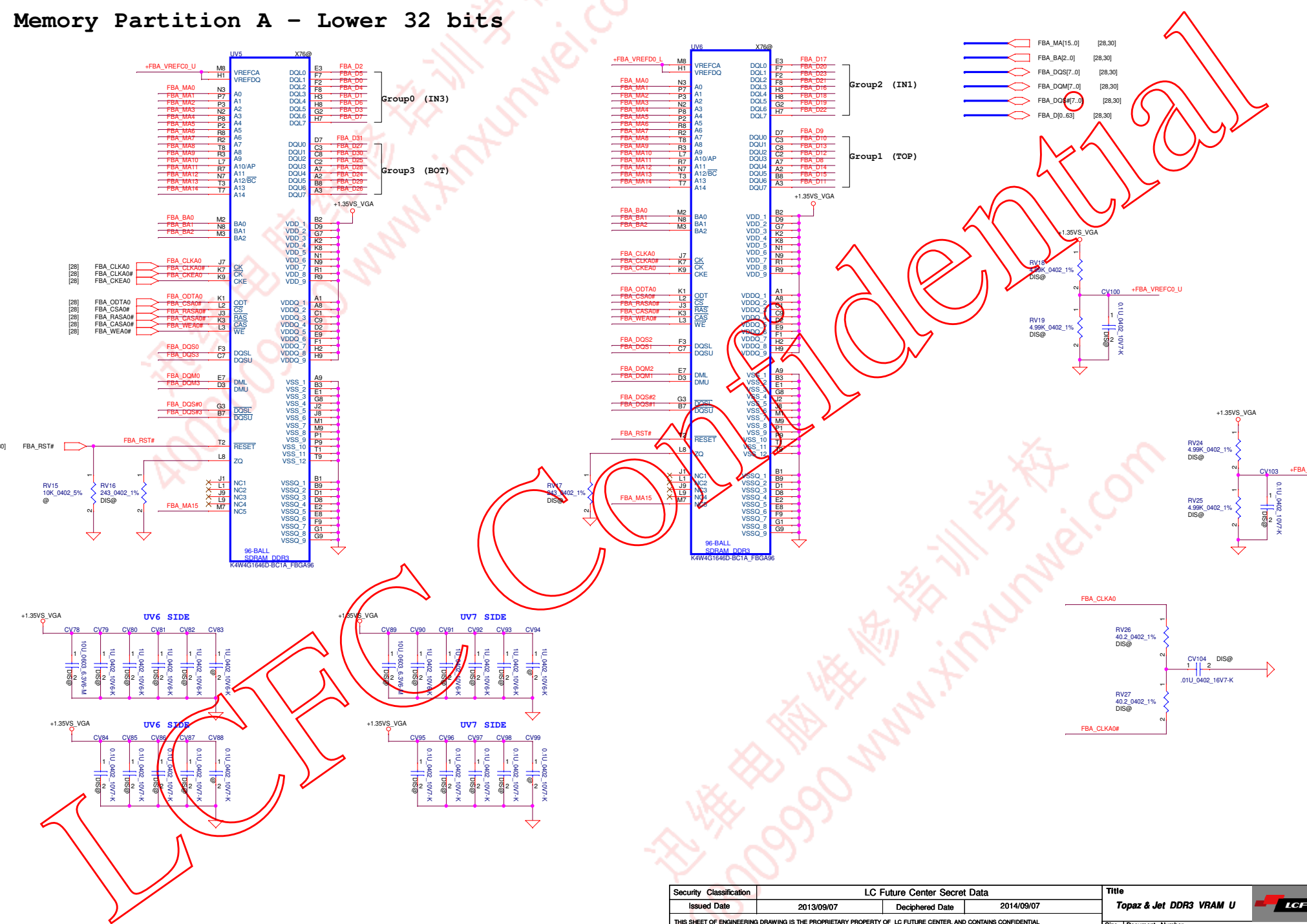




**Memory Partition A - Lower 32 bits**

UV5 X76@

+FBA\_VREFC0\_U M8 VREFCA FBA\_D2 E3 FBA\_D5 F7 FBA\_D8 F9 FBA\_D10 F12 FBA\_D11 F13 FBA\_D12 F14 FBA\_D13 F15 FBA\_D14 F16 FBA\_D15 F17 FBA\_D16 F18 FBA\_D17 F19 FBA\_D18 F20 FBA\_D19 F21 FBA\_D20 F22 FBA\_D21 F23 FBA\_D22 F24 FBA\_D23 F25 FBA\_D24 F26 FBA\_D25 F27 FBA\_D26 F28 FBA\_D27 F29 FBA\_D28 F30 FBA\_D29 F31 FBA\_D30 F32 FBA\_D31 F33 FBA\_D32 F34 FBA\_D33 F35 FBA\_D34 F36 FBA\_D35 F37 FBA\_D36 F38 FBA\_D37 F39 FBA\_D38 F40 FBA\_D39 F41 FBA\_D40 F42 FBA\_D41 F43 FBA\_D42 F44 FBA\_D43 F45 FBA\_D44 F46 FBA\_D45 F47 FBA\_D46 F48 FBA\_D47 F49 FBA\_D48 F50 FBA\_D49 F51 FBA\_D50 F52 FBA\_D51 F53 FBA\_D52 F54 FBA\_D53 F55 FBA\_D54 F56 FBA\_D55 F57 FBA\_D56 F58 FBA\_D57 F59 FBA\_D58 F60 FBA\_D59 F61 FBA\_D60 F62 FBA\_D61 F63 FBA\_D62 F64 FBA\_D63 F65 FBA\_D64 F66 FBA\_D65 F67 FBA\_D66 F68 FBA\_D67 F69 FBA\_D68 F70 FBA\_D69 F71 FBA\_D70 F72 FBA\_D71 F73 FBA\_D72 F74 FBA\_D73 F75 FBA\_D74 F76 FBA\_D75 F77 FBA\_D76 F78 FBA\_D77 F79 FBA\_D78 F80 FBA\_D79 F81 FBA\_D80 F82 FBA\_D81 F83 FBA\_D82 F84 FBA\_D83 F85 FBA\_D84 F86 FBA\_D85 F87 FBA\_D86 F88 FBA\_D87 F89 FBA\_D88 F90 FBA\_D89 F91 FBA\_D90 F92 FBA\_D91 F93 FBA\_D92 F94 FBA\_D93 F95 FBA\_D94 F96 FBA\_D95 F97 FBA\_D96 F98 FBA\_D97 F99 FBA\_D98 F100 FBA\_D99 F101 FBA\_D100 F102 FBA\_D101 F103 FBA\_D102 F104 FBA\_D103 F105 FBA\_D104 F106 FBA\_D105 F107 FBA\_D106 F108 FBA\_D107 F109 FBA\_D108 F110 FBA\_D109 F111 FBA\_D110 F112 FBA\_D111 F113 FBA\_D112 F114 FBA\_D113 F115 FBA\_D114 F116 FBA\_D115 F117 FBA\_D116 F118 FBA\_D117 F119 FBA\_D118 F120 FBA\_D119 F121 FBA\_D120 F122 FBA\_D121 F123 FBA\_D122 F124 FBA\_D123 F125 FBA\_D124 F126 FBA\_D125 F127 FBA\_D126 F128 FBA\_D127 F129 FBA\_D128 F130 FBA\_D129 F131 FBA\_D130 F132 FBA\_D131 F133 FBA\_D132 F134 FBA\_D133 F135 FBA\_D134 F136 FBA\_D135 F137 FBA\_D136 F138 FBA\_D137 F139 FBA\_D138 F140 FBA\_D139 F141 FBA\_D140 F142 FBA\_D141 F143 FBA\_D142 F144 FBA\_D143 F145 FBA\_D144 F146 FBA\_D145 F147 FBA\_D146 F148 FBA\_D147 F149 FBA\_D148 F150 FBA\_D149 F151 FBA\_D150 F152 FBA\_D151 F153 FBA\_D152 F154 FBA\_D153 F155 FBA\_D154 F156 FBA\_D155 F157 FBA\_D156 F158 FBA\_D157 F159 FBA\_D158 F160 FBA\_D159 F161 FBA\_D160 F162 FBA\_D161 F163 FBA\_D162 F164 FBA\_D163 F165 FBA\_D164 F166 FBA\_D165 F167 FBA\_D166 F168 FBA\_D167 F169 FBA\_D168 F170 FBA\_D169 F171 FBA\_D170 F172 FBA\_D171 F173 FBA\_D172 F174 FBA\_D173 F175 FBA\_D174 F176 FBA\_D175 F177 FBA\_D176 F178 FBA\_D177 F179 FBA\_D178 F180 FBA\_D179 F181 FBA\_D180 F182 FBA\_D181 F183 FBA\_D182 F184 FBA\_D183 F185 FBA\_D184 F186 FBA\_D185 F187 FBA\_D186 F188 FBA\_D187 F189 FBA\_D188 F190 FBA\_D189 F191 FBA\_D190 F192 FBA\_D191 F193 FBA\_D192 F194 FBA\_D193 F195 FBA\_D194 F196 FBA\_D195 F197 FBA\_D196 F198 FBA\_D197 F199 FBA\_D198 F200 FBA\_D199 F201 FBA\_D200 F202 FBA\_D201 F203 FBA\_D202 F204 FBA\_D203 F205 FBA\_D204 F206 FBA\_D205 F207 FBA\_D206 F208 FBA\_D207 F209 FBA\_D208 F210 FBA\_D209 F211 FBA\_D210 F212 FBA\_D211 F213 FBA\_D212 F214 FBA\_D213 F215 FBA\_D214 F216 FBA\_D215 F217 FBA\_D216 F218 FBA\_D217 F219 FBA\_D218 F220 FBA\_D219 F221 FBA\_D220 F222 FBA\_D221 F223 FBA\_D222 F224 FBA\_D223 F225 FBA\_D224 F226 FBA\_D225 F227 FBA\_D226 F228 FBA\_D227 F229 FBA\_D228 F230 FBA\_D229 F231 FBA\_D230 F232 FBA\_D231 F233 FBA\_D232 F234 FBA\_D233 F235 FBA\_D234 F236 FBA\_D235 F237 FBA\_D236 F238 FBA\_D237 F239 FBA\_D238 F240 FBA\_D239 F241 FBA\_D240 F242 FBA\_D241 F243 FBA\_D242 F244 FBA\_D243 F245 FBA\_D244 F246 FBA\_D245 F247 FBA\_D246 F248 FBA\_D247 F249 FBA\_D248 F250 FBA\_D249 F251 FBA\_D250 F252 FBA\_D251 F253 FBA\_D252 F254 FBA\_D253 F255 FBA\_D254 F256 FBA\_D255 F257 FBA\_D256 F258 FBA\_D257 F259 FBA\_D258 F260 FBA\_D259 F261 FBA\_D260 F262 FBA\_D261 F263 FBA\_D262 F264 FBA\_D263 F265 FBA\_D264 F266 FBA\_D265 F267 FBA\_D266 F268 FBA\_D267 F269 FBA\_D268 F270 FBA\_D269 F271 FBA\_D270 F272 FBA\_D271 F273 FBA\_D272 F274 FBA\_D273 F275 FBA\_D274 F276 FBA\_D275 F277 FBA\_D276 F278 FBA\_D277 F279 FBA\_D278 F280 FBA\_D279 F281 FBA\_D280 F282 FBA\_D281 F283 FBA\_D282 F284 FBA\_D283 F285 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F352 FBA\_D351 F353 FBA\_D352 F354 FBA\_D353 F355 FBA\_D354 F356 FBA\_D355 F357 FBA\_D356 F358 FBA\_D357 F359 FBA\_D358 F360 FBA\_D359 F361 FBA\_D360 F362 FBA\_D361 F363 FBA\_D362 F364 FBA\_D363 F365 FBA\_D364 F366 FBA\_D365 F367 FBA\_D366 F368 FBA\_D367 F369 FBA\_D368 F370 FBA\_D369 F371 FBA\_D370 F372 FBA\_D371 F373 FBA\_D372 F374 FBA\_D373 F375 FBA\_D374 F376 FBA\_D375 F377 FBA\_D376 F378 FBA\_D377 F379 FBA\_D378 F380 FBA\_D379 F381 FBA\_D380 F382 FBA\_D381 F383 FBA\_D382 F384 FBA\_D383 F385 FBA\_D384 F386 FBA\_D385 F387 FBA\_D386 F388 FBA\_D387 F389 FBA\_D388 F390 FBA\_D389 F391 FBA\_D390 F392 FBA\_D391 F393 FBA\_D392 F394 FBA\_D393 F395 FBA\_D394 F396 FBA\_D395 F397 FBA\_D396 F398 FBA\_D397 F399 FBA\_D398 F400 FBA\_D399 F401 FBA\_D400 F402 FBA\_D401 F403 FBA\_D402 F404 FBA\_D403 F405 FBA\_D404 F406 FBA\_D405 F407 FBA\_D406 F408 FBA\_D407 F409 FBA\_D408 F410 FBA\_D409 F411 FBA\_D410 F412 FBA\_D411 F413





**Security Classification**

LC Future Center Secret Data

**Title**

Topaz & Jet DDR3 VRAM L

**Issued Date**

2013/09/07

**Deciphered Date**

2014/09/07

**Size**

Custom

**Document Number**

BE460 NW-A551

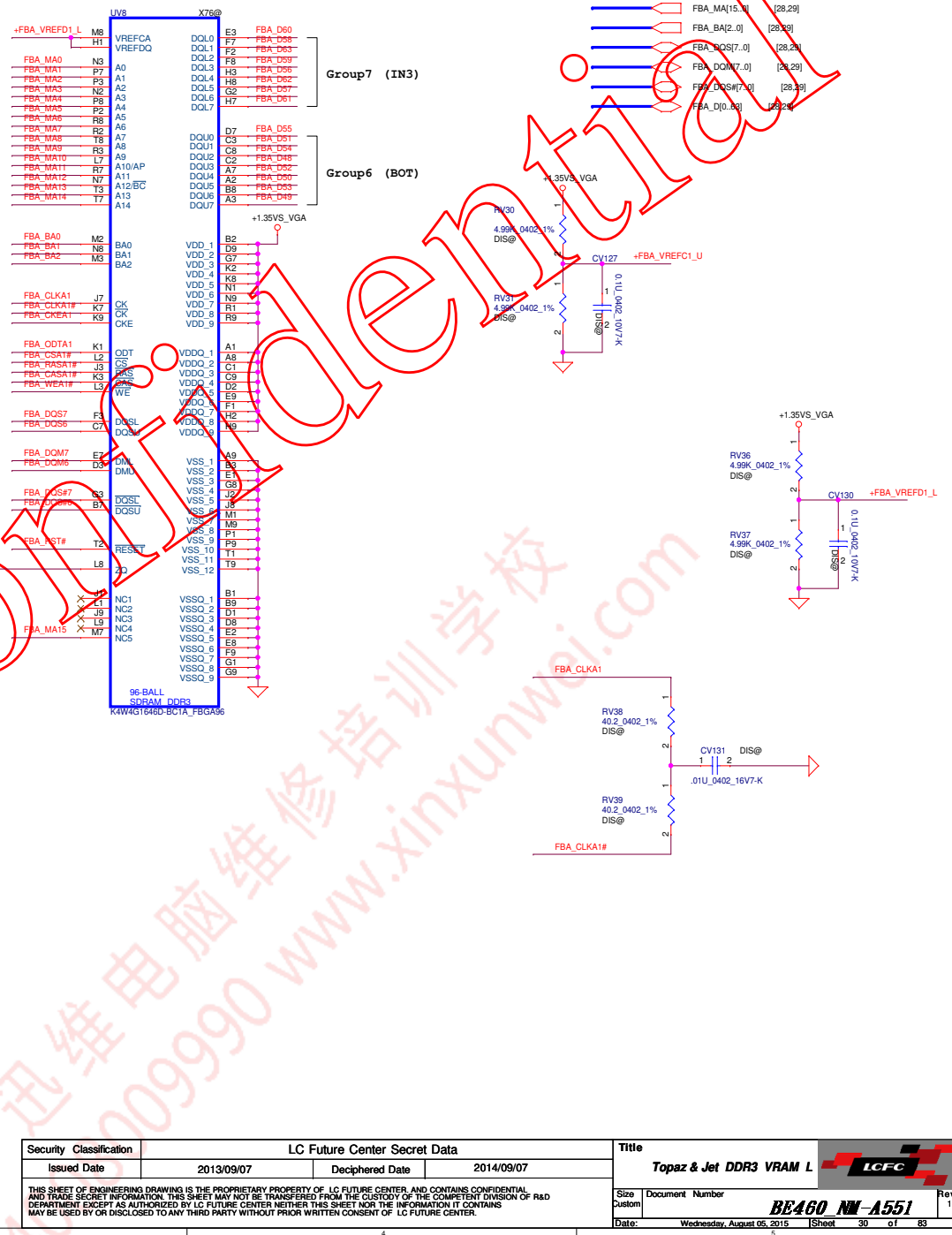
**Date**


Wednesday, August 05, 2015

**Sheet**

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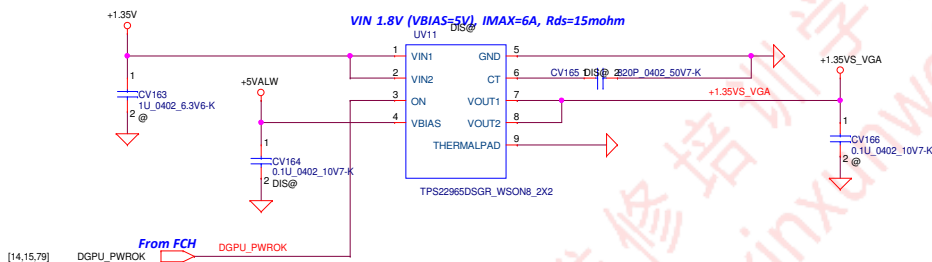
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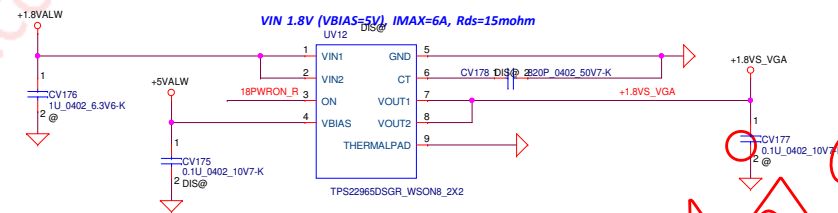
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# +1.35V to +1.35VS\_VGA

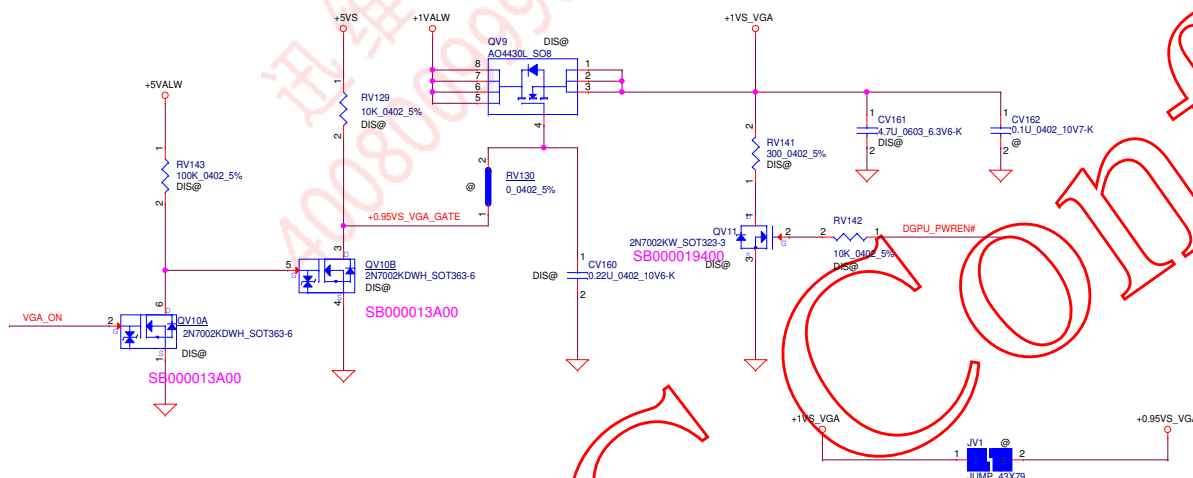


# +1.8VALW to +1.8VS\_VGA

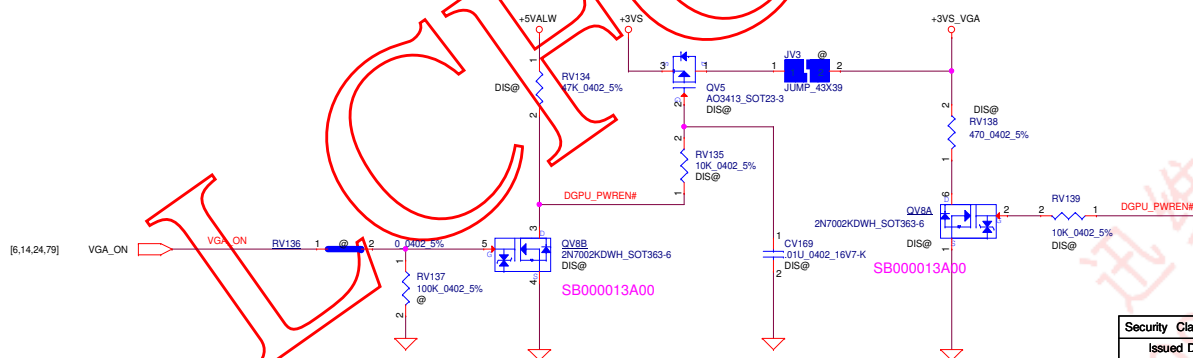


MLPS	Bit				
	5	4	3	2	1
PS_0[5:1]	1	1	0	0	1
PS_1[5:1]	1	1	0	0	0
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X

# +1VALW to +1VS\_VGA




# +3VS to +3VS\_VGA



PS_0[1]	ROM_CONFIG[0]	STRAP BIOS_ROM_EN = 1
PS_0[2]	ROM_CONFIG[1]	ROM_CONFIG[2:0] = [001] 256MB
PS_0[3]	ROM_CONFIG[2]	
PS_0[4]	N/A	1 (Default)
PS_0[5]	N/A	1 (Default)
PS_1[1]	STRAP_BIF_GEN3_EN_A	0 = PCIe GEN3 is not supported
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled
PS_1[3]	N/A	0 (Default)
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	1 = Tx deemphasis enabled
PS_2[1]	N/A	0 (Default)
PS_2[2]	N/A	0 (Default)
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device
PS_2[4]	N/A	1 (Default)
PS_2[5]	N/A	1 (Default)
PS_3[1]	BOARD_CONFIG[0]	PS_3[3..1]
PS_3[2]	BOARD_CONFIG[1]	101 = Micron 2G
PS_3[3]	BOARD_CONFIG[2]	110 = Samsung 2G
		111 = Hynix 2G
PS_3[4]	N/A	1 (Default)
PS_3[5]	N/A	1 (Default)

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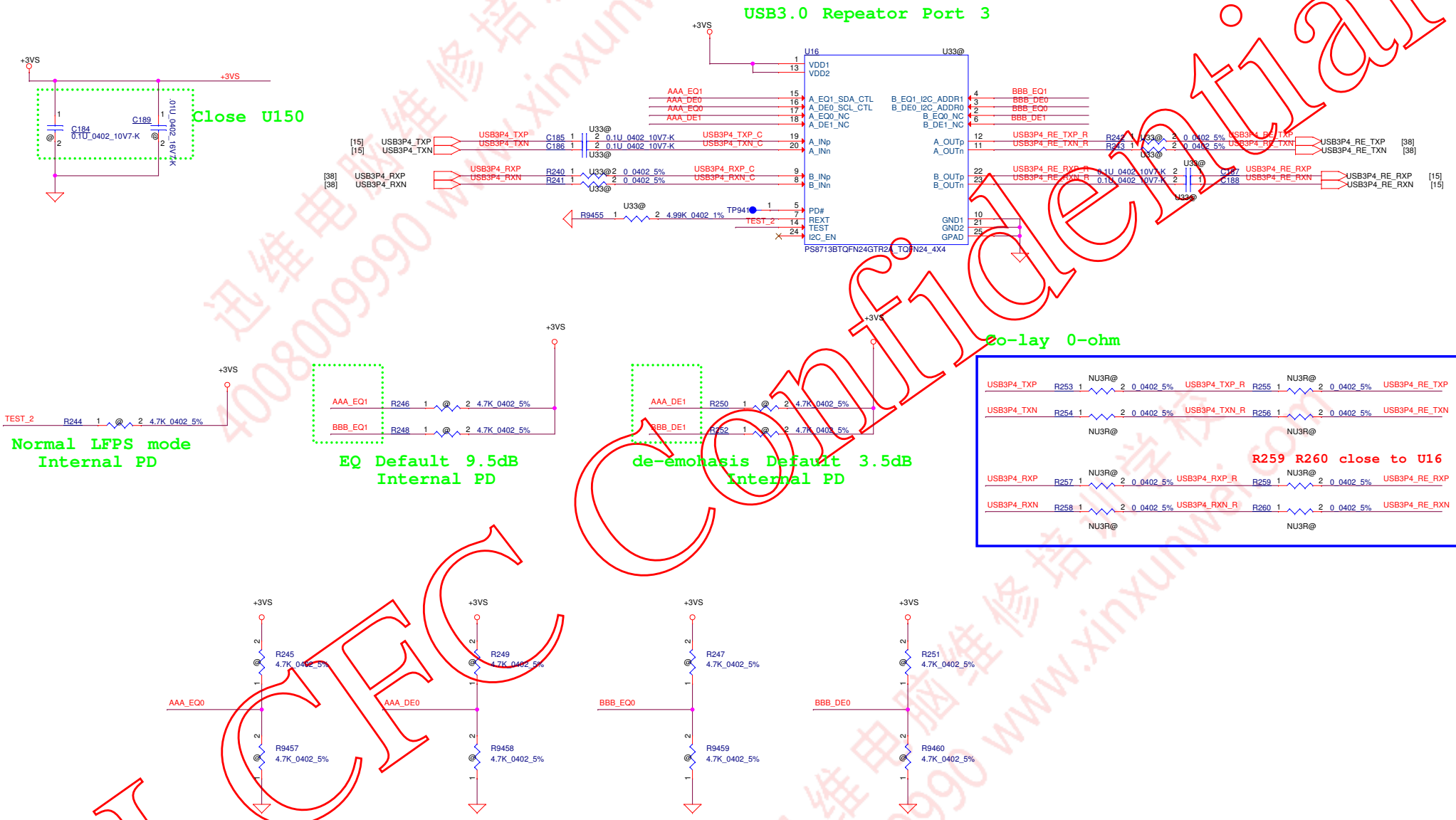
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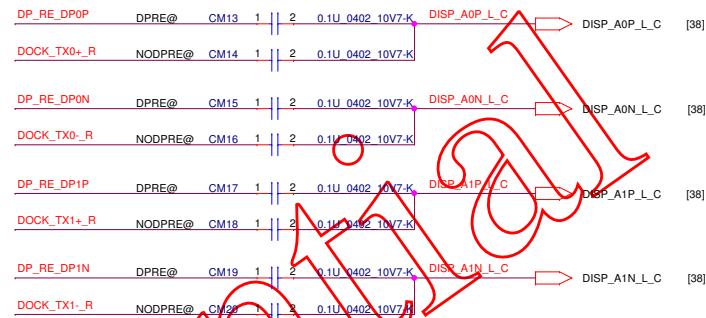
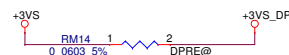


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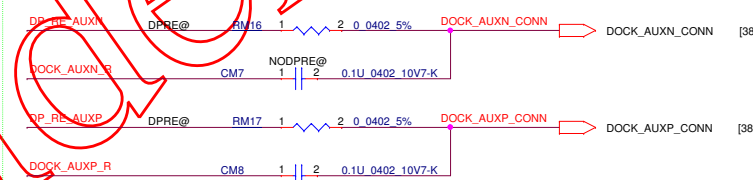
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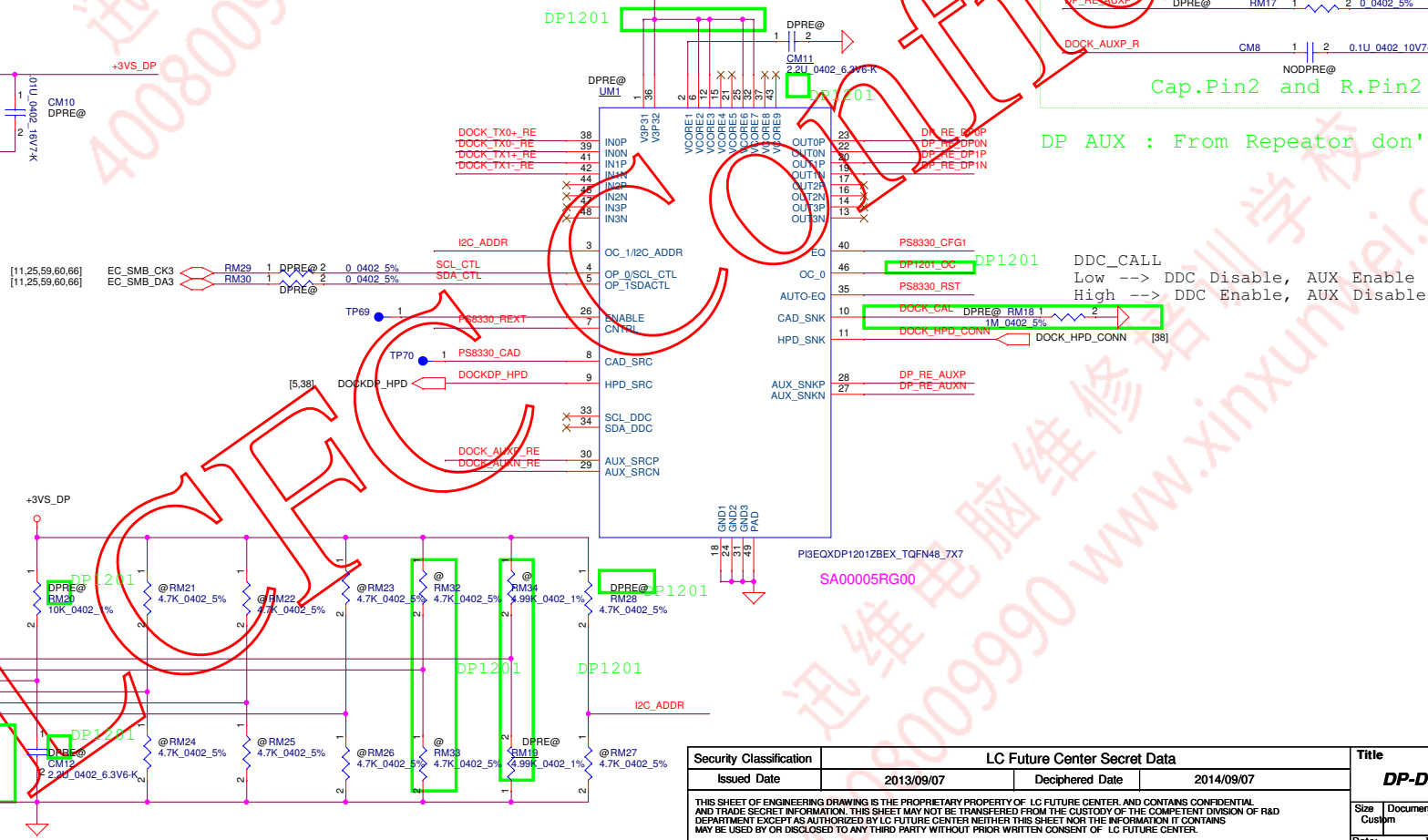


## R.Pin2 and R.Pin2 Co-lay




Cap.Pin2 and R.Pin2 Co-lay

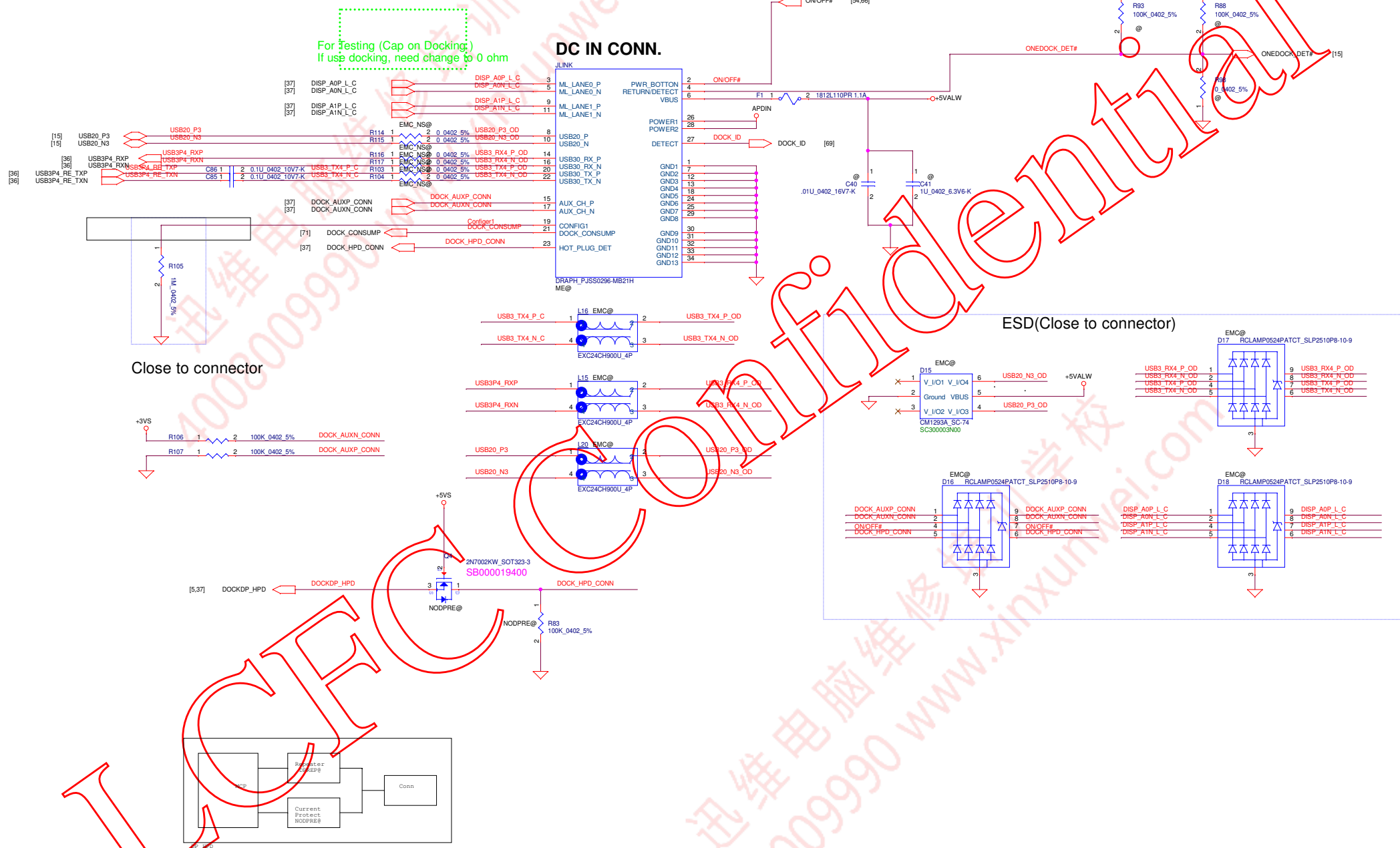
DP AUX : From Repeater don't need cap, but PCH.

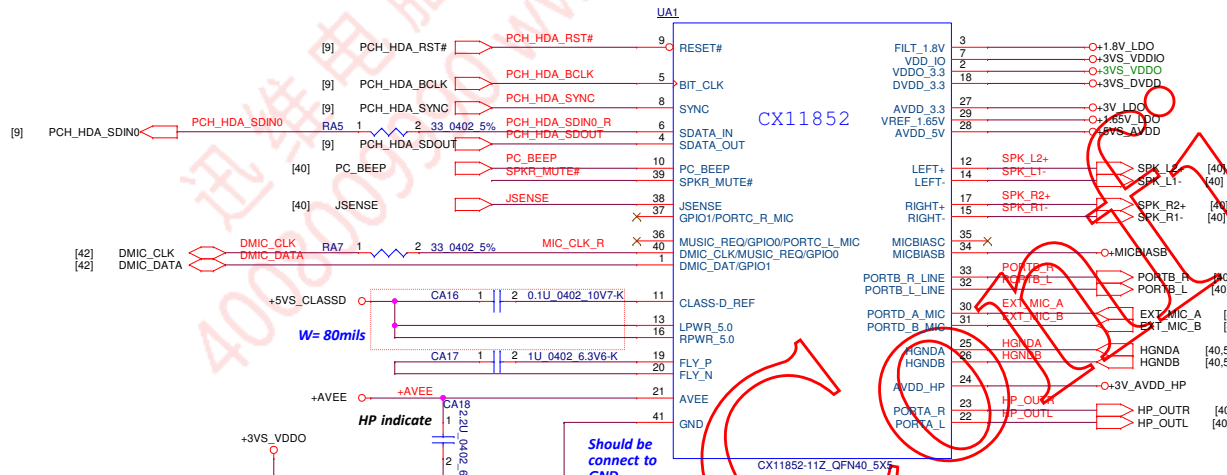
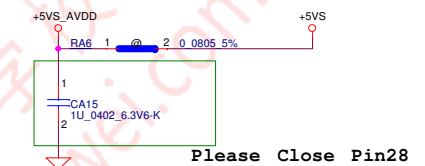
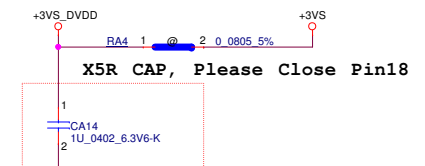
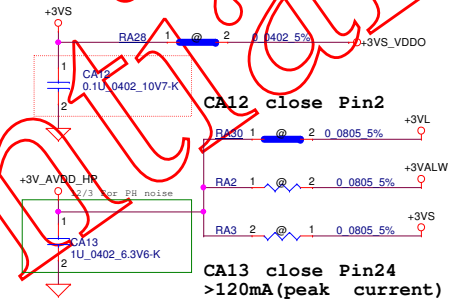
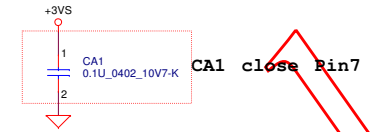
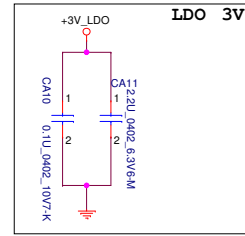
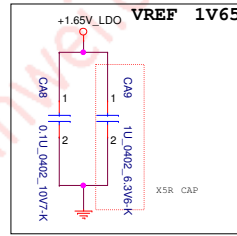
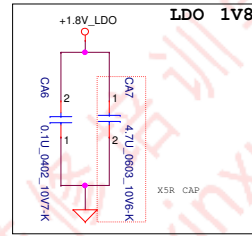
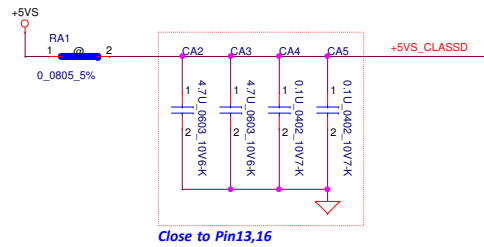


2015, 01, 02

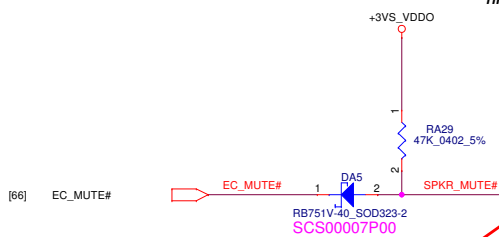
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Title			
<b>DP-DOCKING RP</b>			
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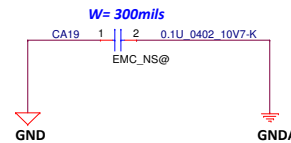




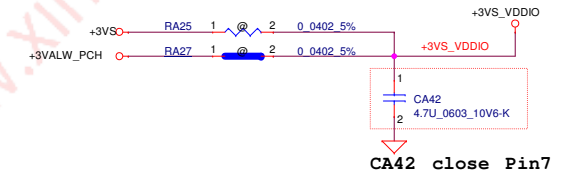
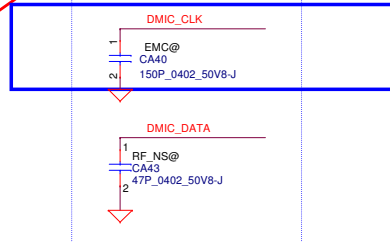
Apple --> EXT\_MIC\_A, HGND\_B  
Nokia --> EXT\_MIC\_B, HGND\_A  
HGND\_A/HGND\_B trace widths should be as wide as possible



Should be connect to GND



RF, close to RA7  
Close to RA7 (as RC filter)

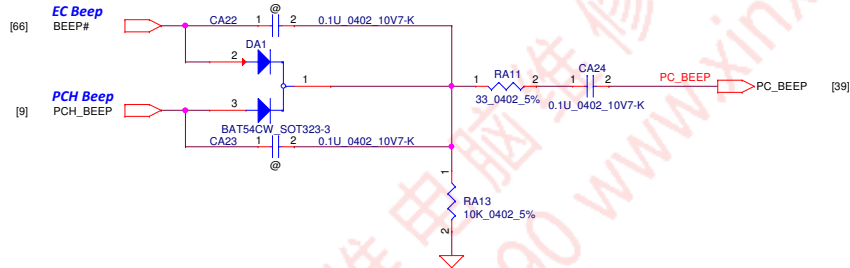


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CX11852 & SPEAKER					
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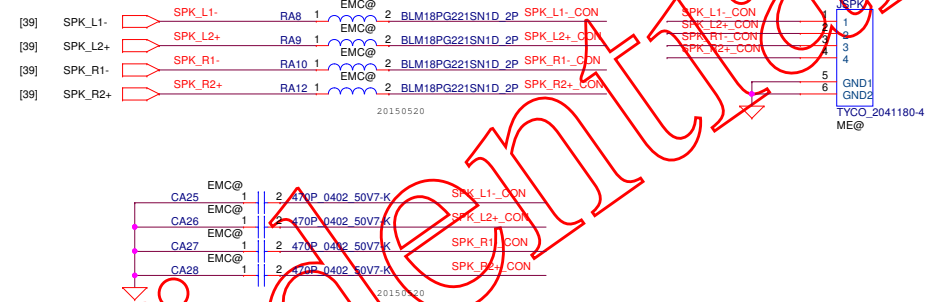


## PC BEEP



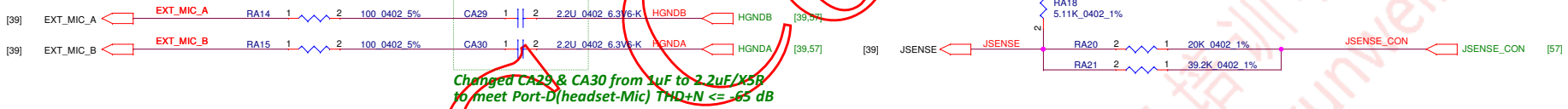
## Speaker OUT

## SPK CONN.

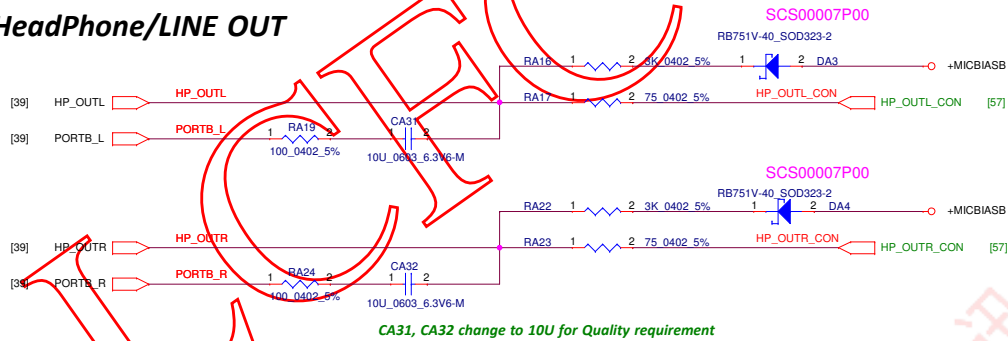



## EXT. MIC/LINE IN

Apple --> EXT\_MIC\_A, HGND B  
Nokia --> EXT\_MIC\_B, HGND A



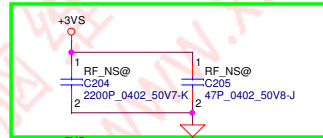
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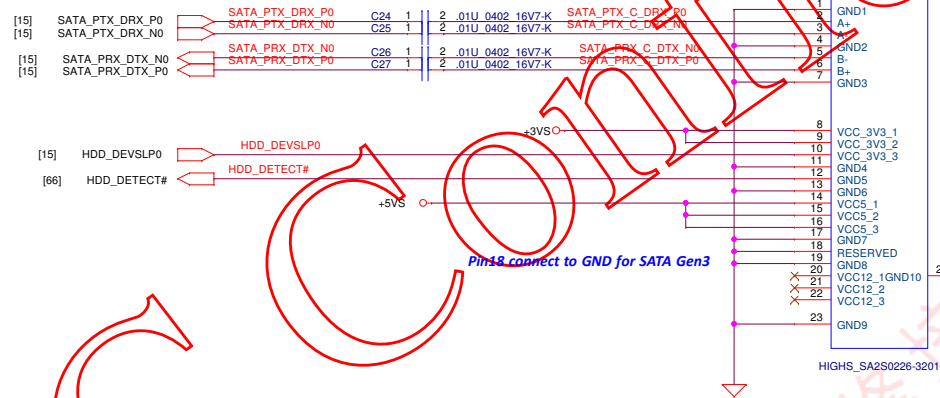
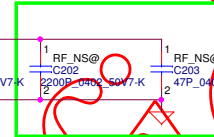
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# SATA HDD CONN.

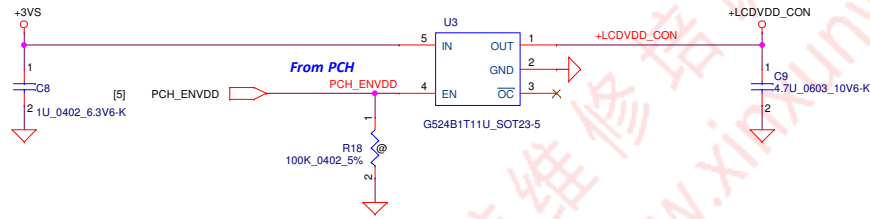
Close to JHDD



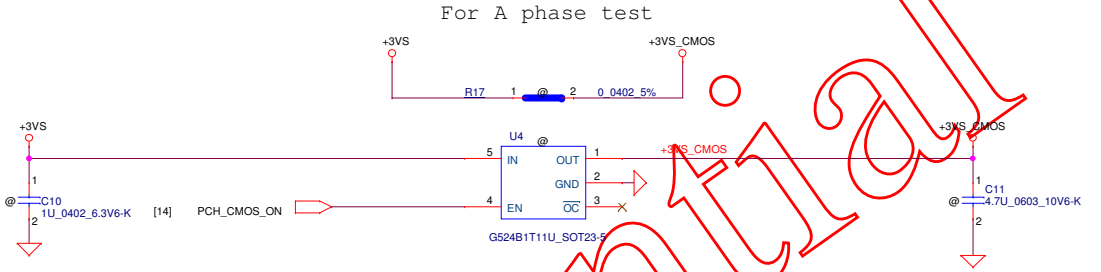
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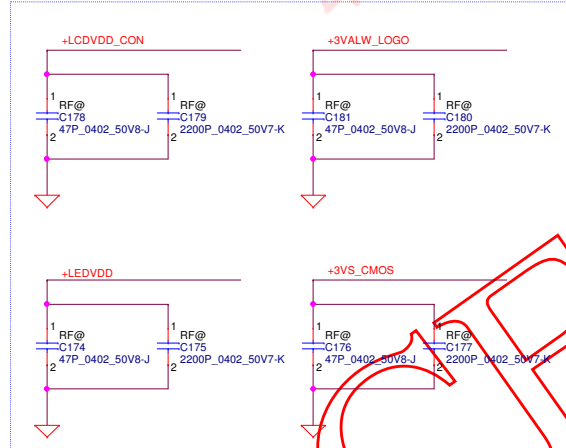
# LCDVDD Circuit



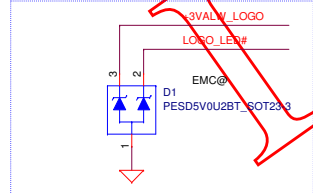
# CMOS Camera



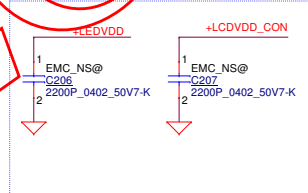
# RF



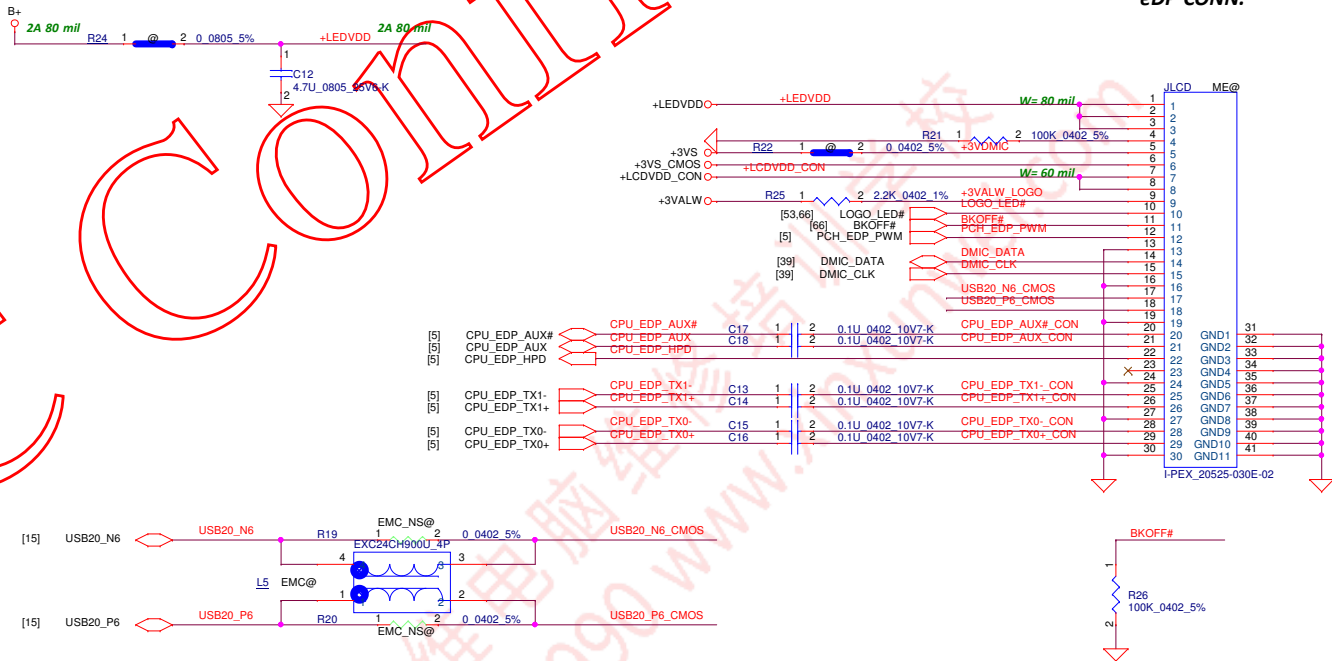
# ESD request




# EMC request, Close to JLCD



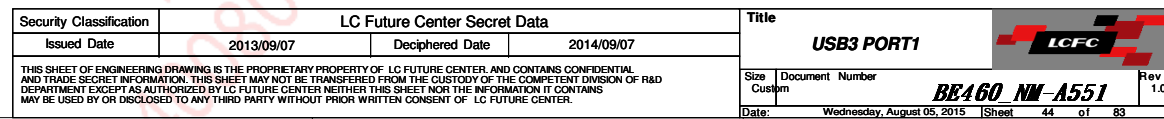
# eDP CONN.



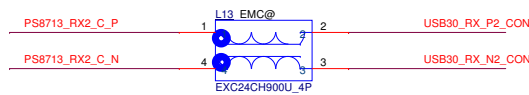
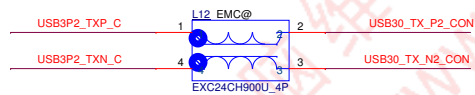
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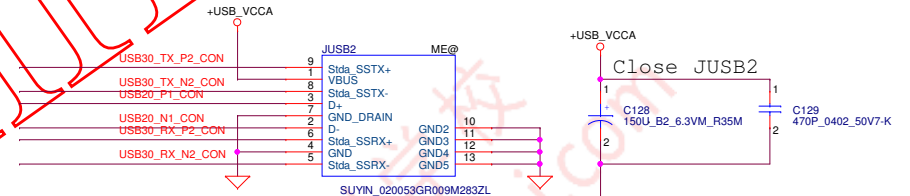
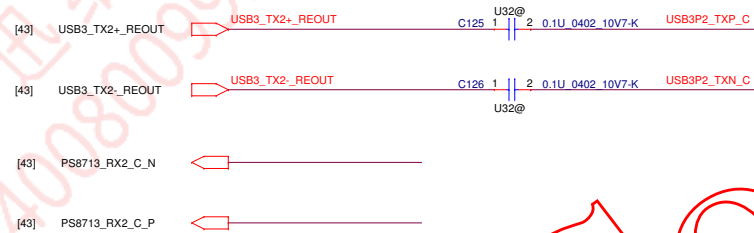
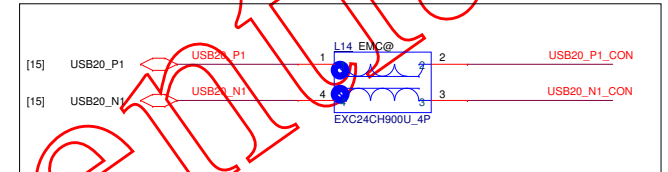
For 14" use(14" on board USB don't support S&C  
,But 15" on board USB support S&C.S&C IC always on MB)



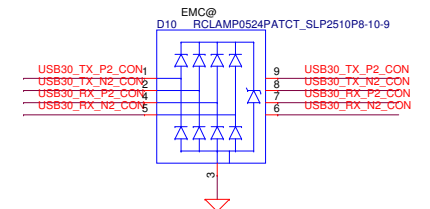
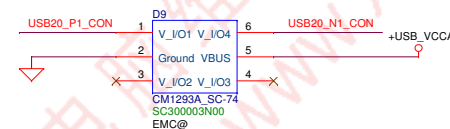
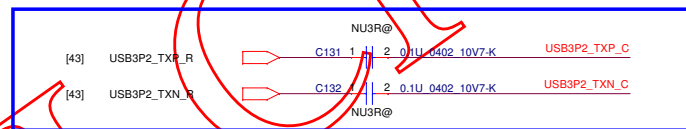




Co-layout L15 for EMI test




Co-lay 0-ohm





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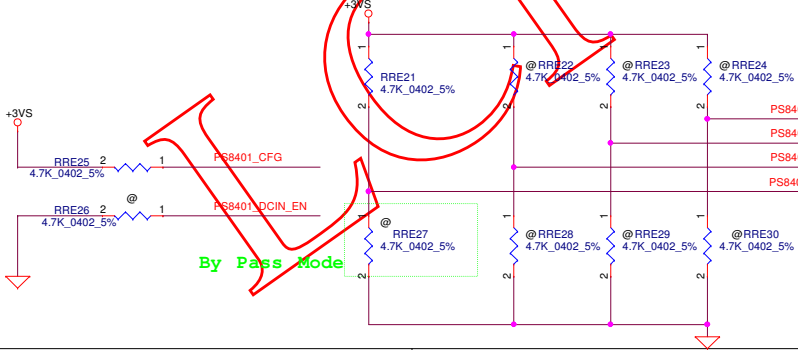
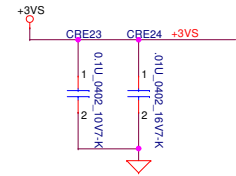
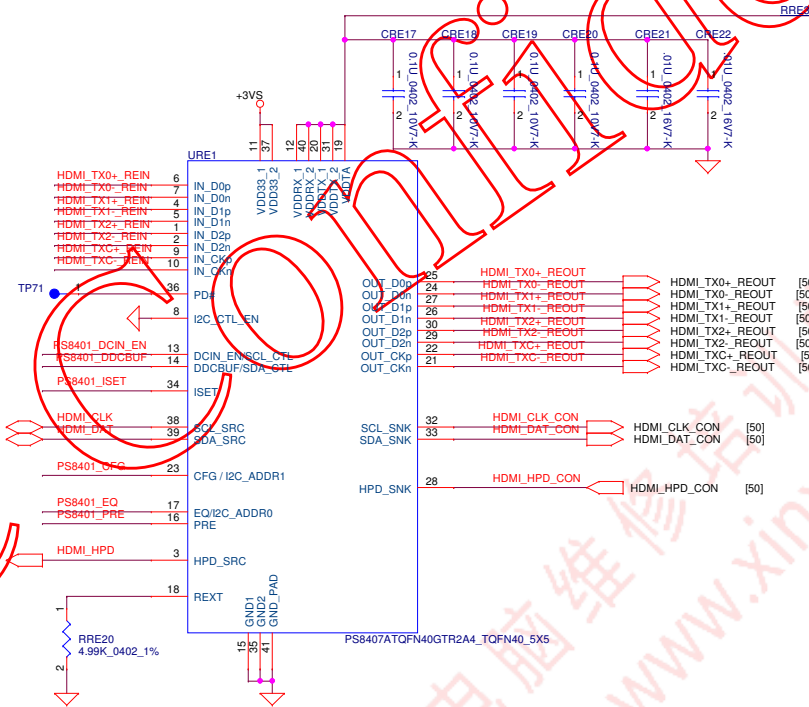
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## HDMI Repeater

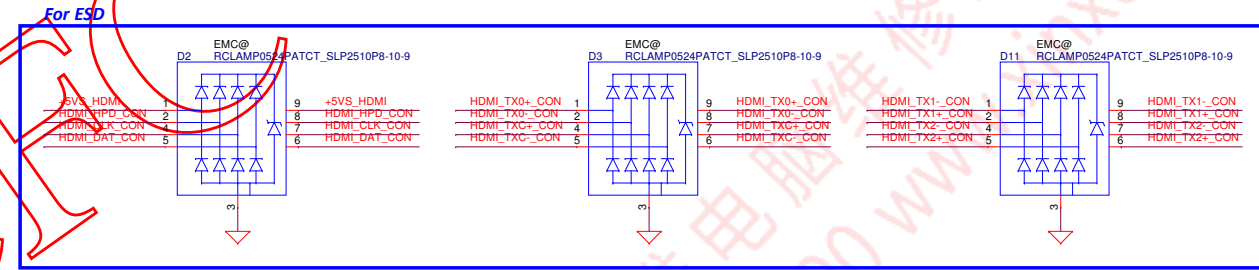
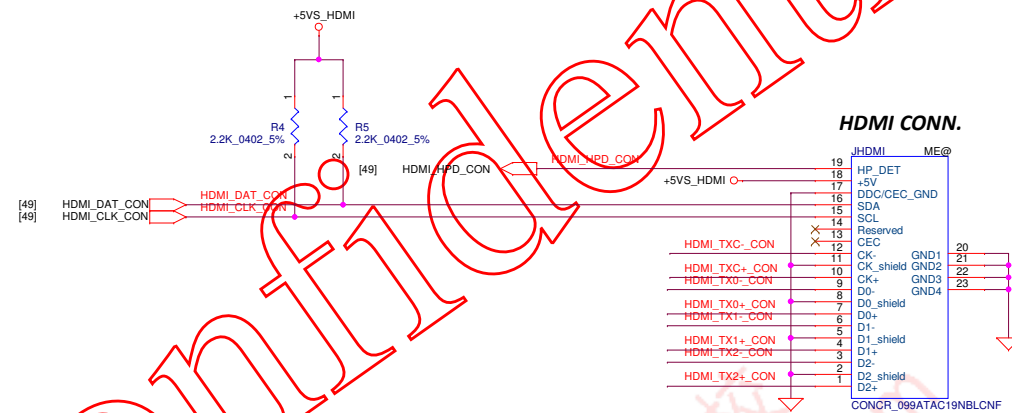
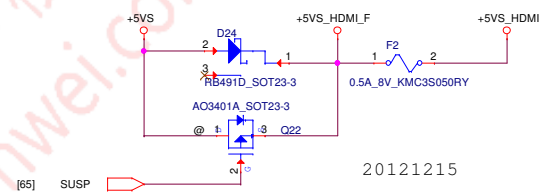
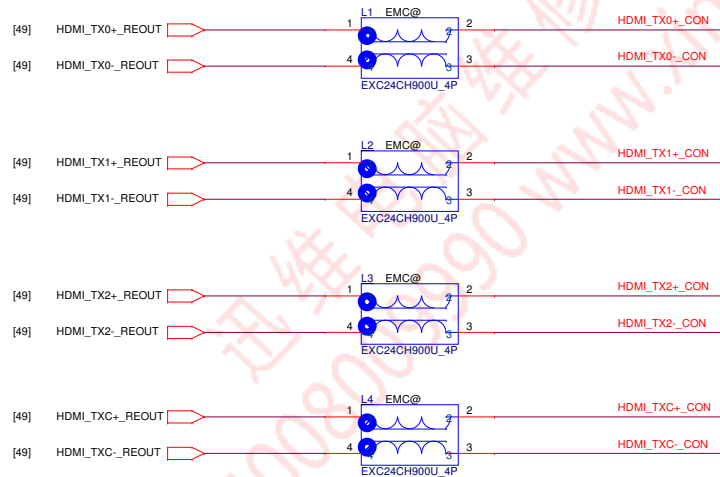


For 8407 use

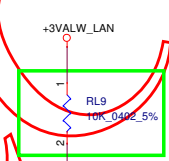
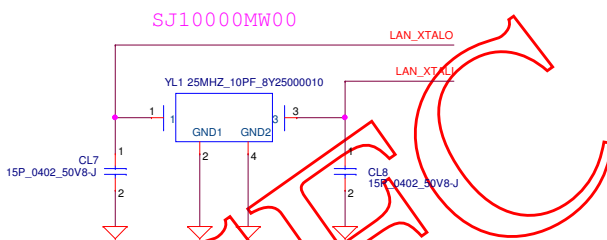
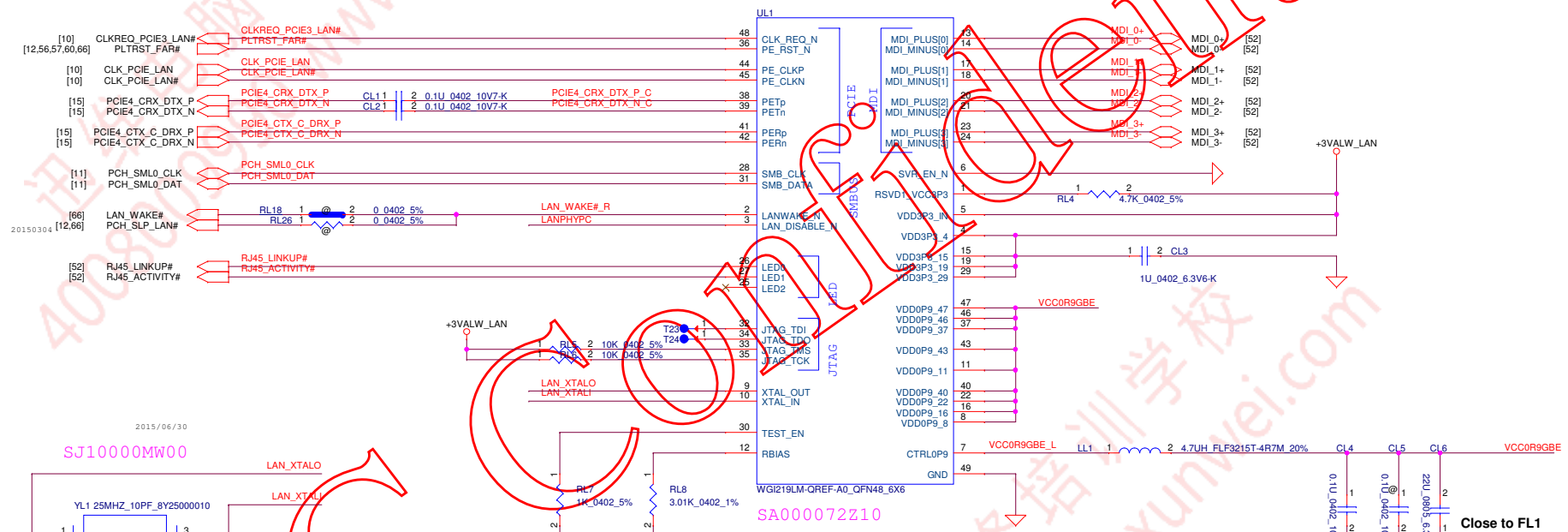
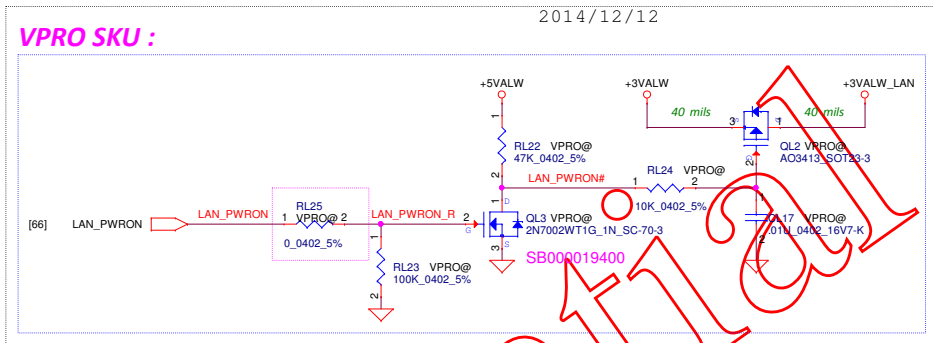


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Custom					1.0
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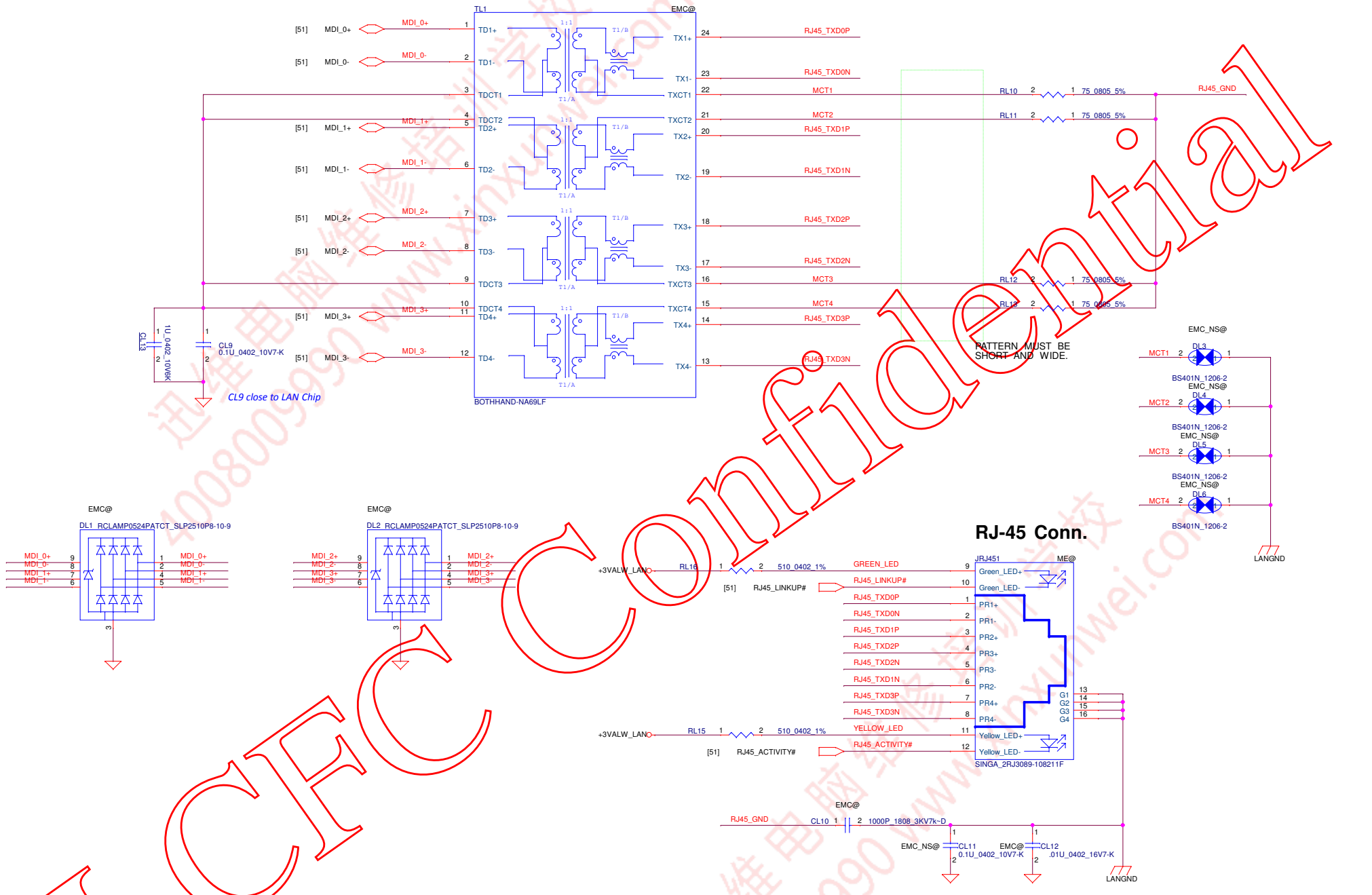


When use Native function, intel recommend pull high 10K ohm  
This part is un-mount in Sting.

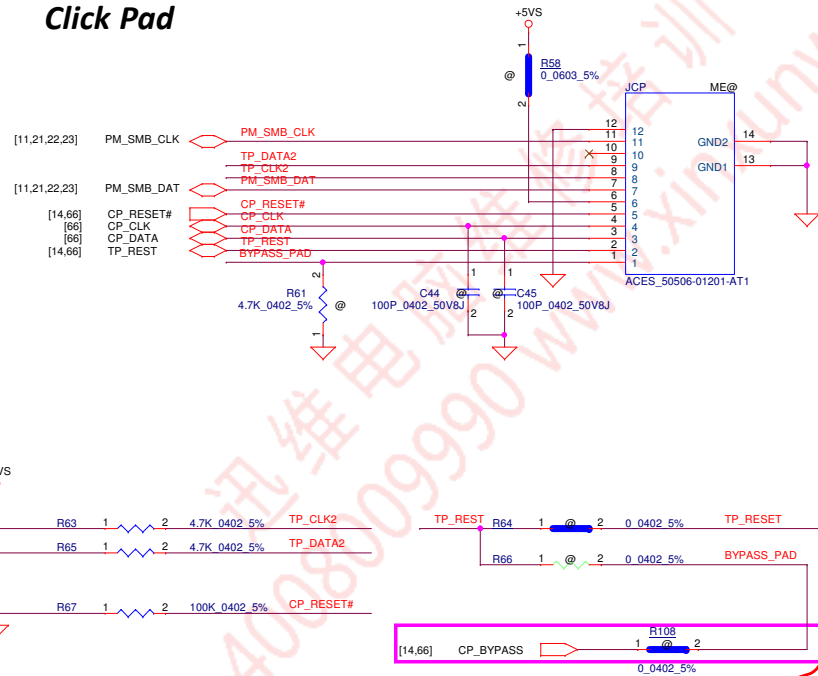
UL1 GBE PHY

vPro Model	Non-vPro Model
WG1219LM	WG1219V
SA000073000	SA000072Z10 SA000072Z20

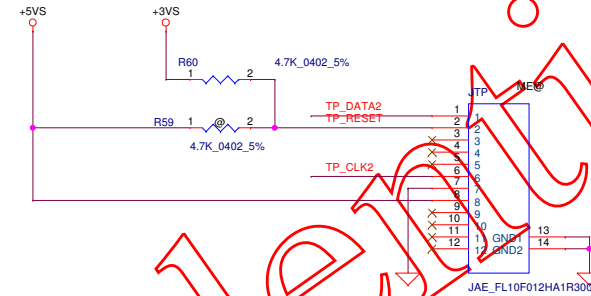
ST-1\_SWG\_SDV-SWG\_EC062  
Add vPro/Non-vPro table.



## Click Pad



## Track point

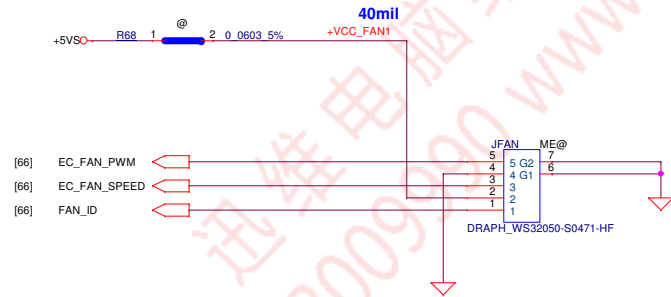


Only for Edge 14"

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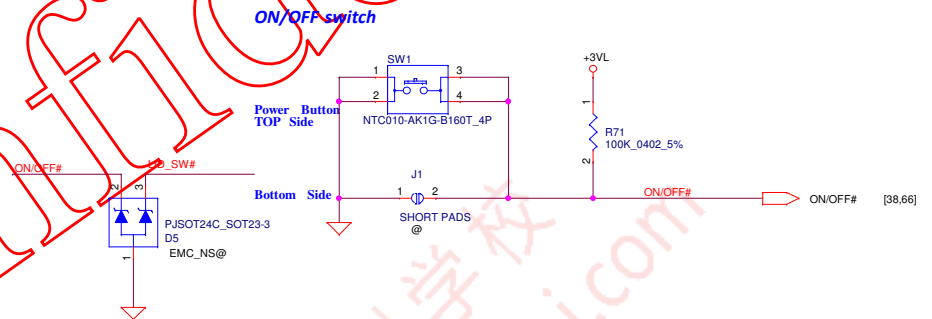


## FAN CONN.



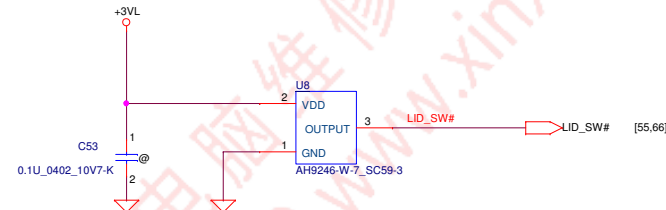
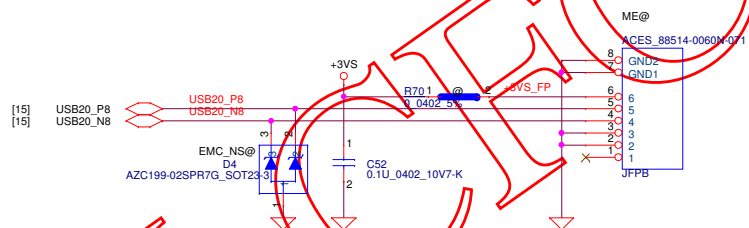
## PWR BTN/LID SW CONN.


For 14" on board  
For 15" on Sub/B

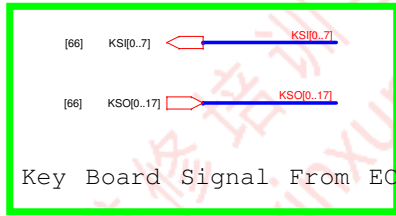


## Lid Switch

## FingerPrint CONN.

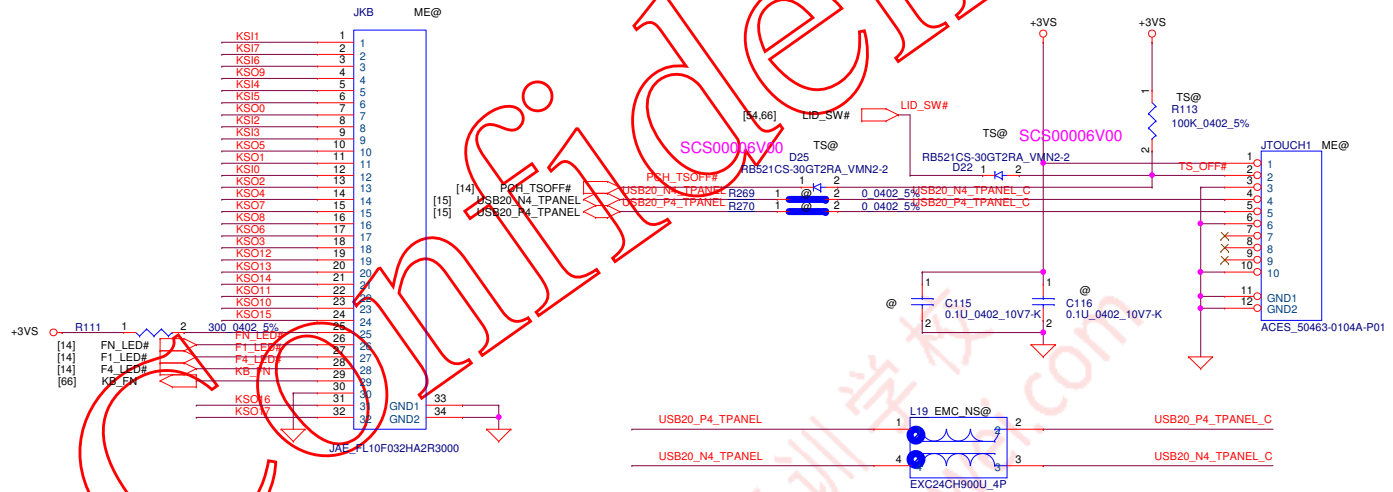
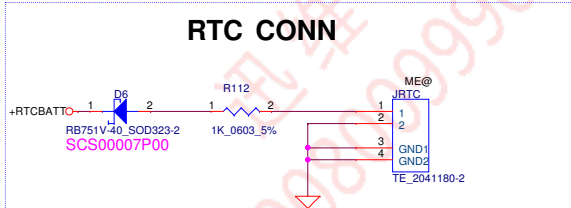


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KeyBoard CONN.(14")

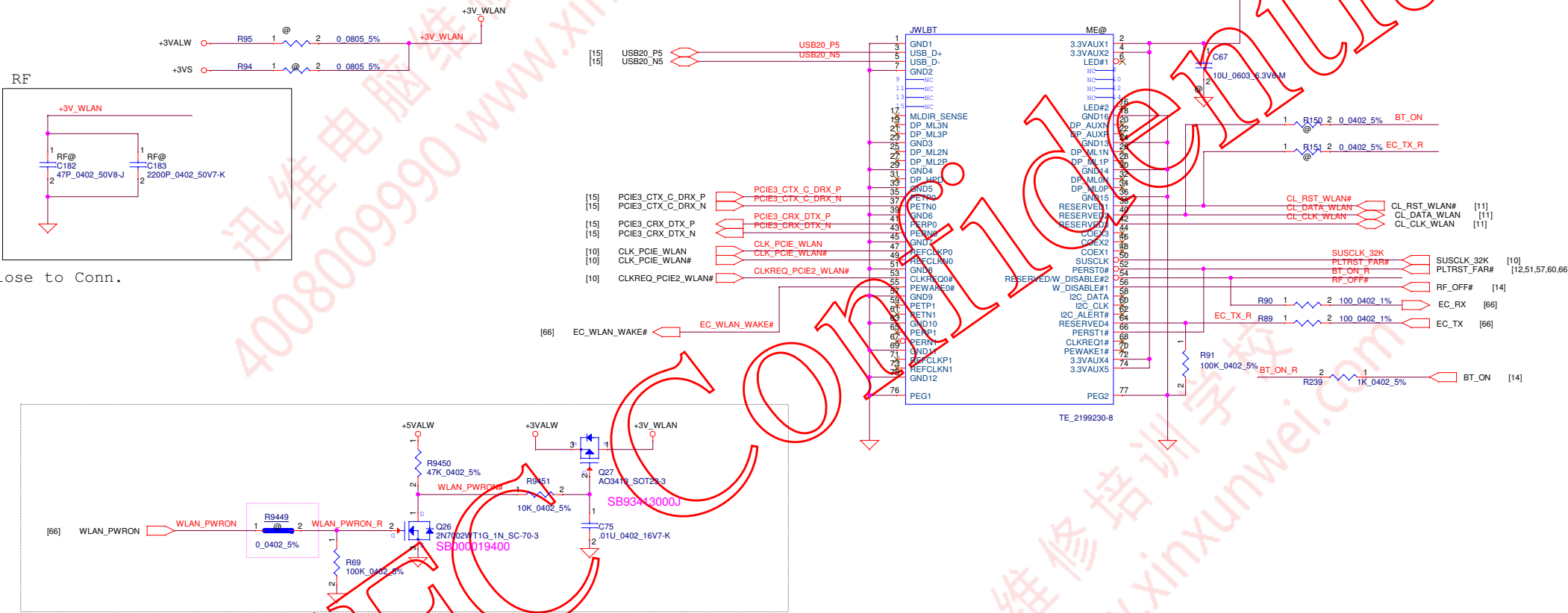
Touch Panel CONN. For 14"



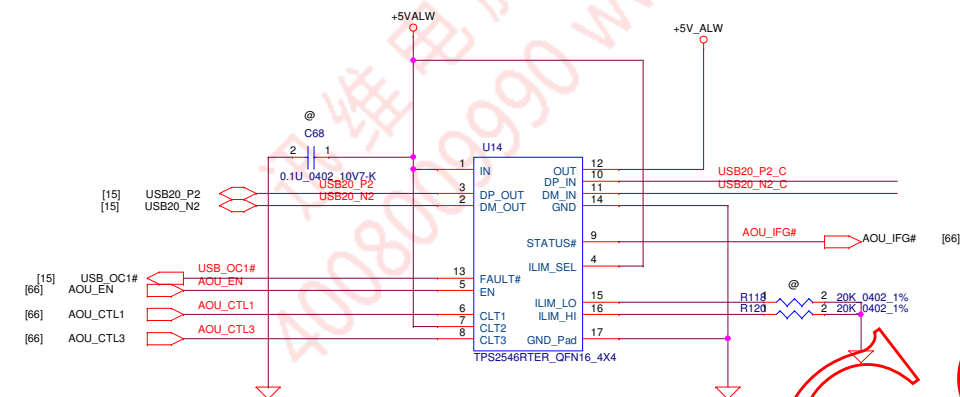
LCFC

# TYPE-A NGFF CCARD FOR WLAN

## 3.2H CONNECTOR



For 14" S&C IC on MB) S&C port on SUB/B

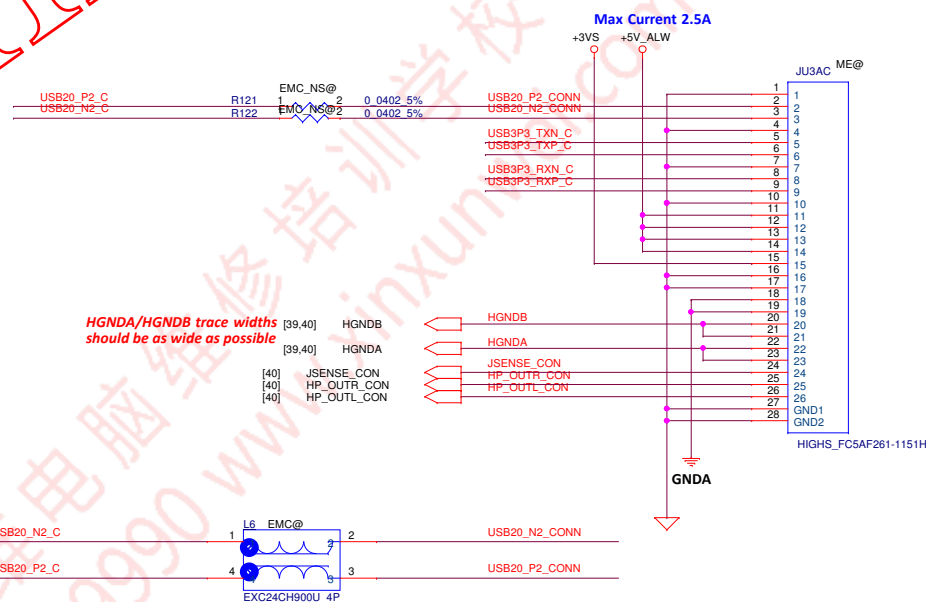
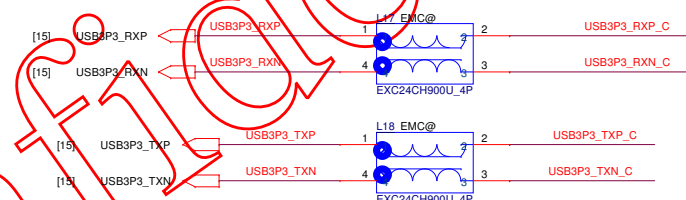
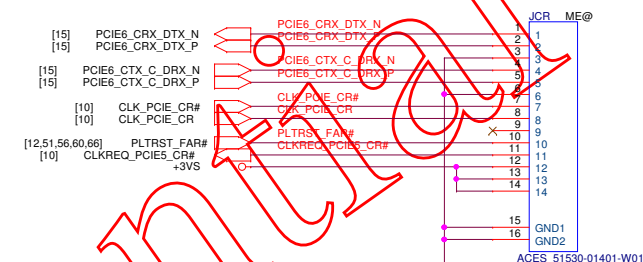


# TI TPS2546

CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCH OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP Bc 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active

USB\_OC5# to MCP  
AOU\_EN to EC  
AOU\_CTL1 to EC  
AOU\_CTL3 to EC  
AOU\_IFG# to EC


For 14" CardReader Board : FFC



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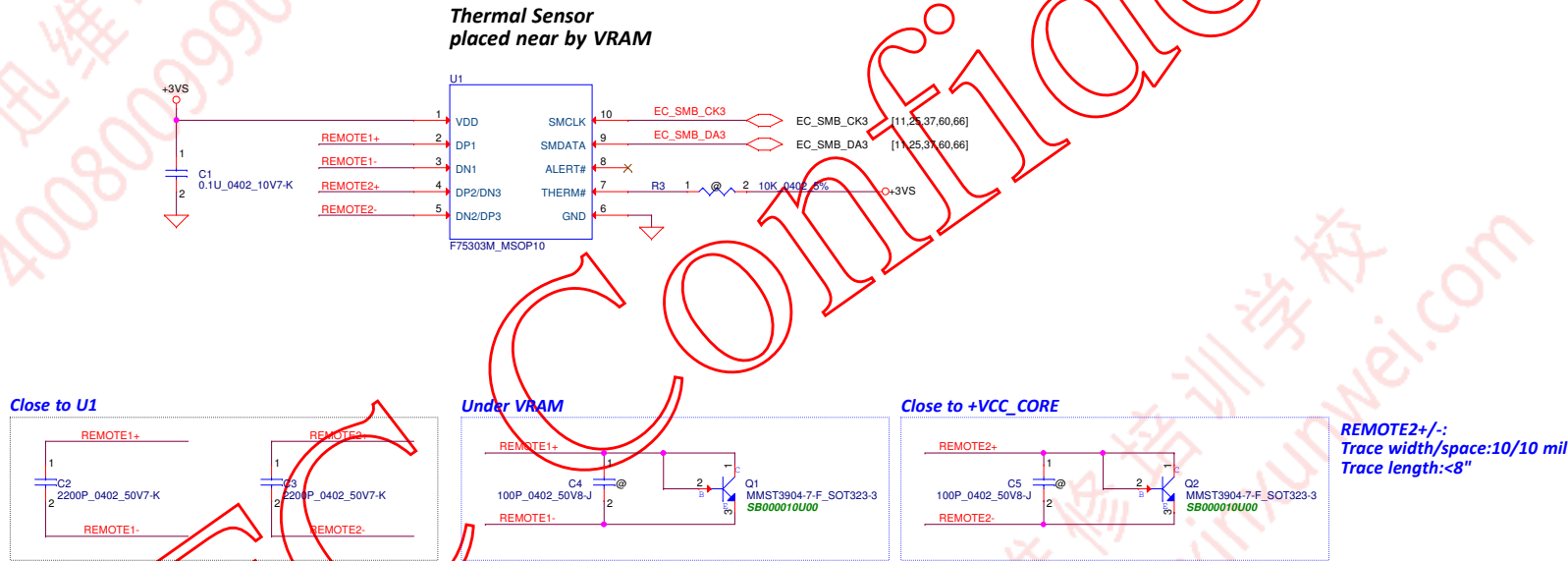
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迅维电脑维修培训学校  
4008009990 www.xinxunwei.com

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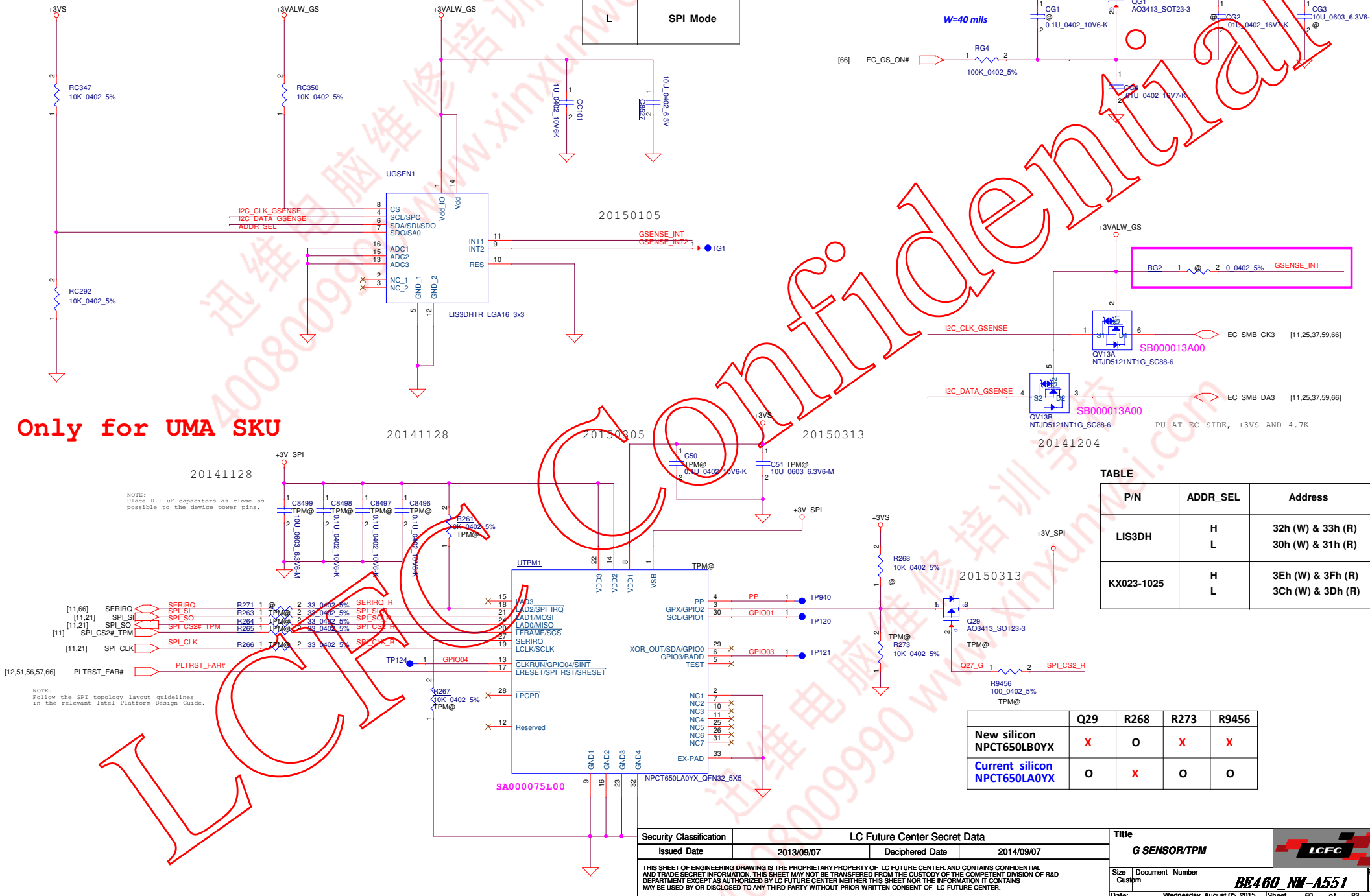


Thermal Sensor



APS G-Sensor

TABLE	
P/N	Mode Selection
H	I2C Mode
L	SPI Mode




Only for UMA SKU


TABLE		
P/N	ADDR_SEL	Address
LIS3DH	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

	Q29	R268	R273	R9456
New silicon NPCT650LB0YX	X	O	X	X
Current silicon NPCT650LA0YX	O	X	O	O

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+1VALW to +VCC\_IO\_AP

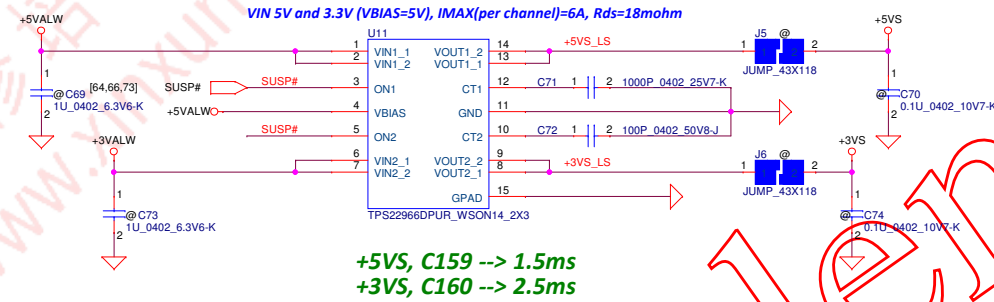
3 A

20150522  
20150714

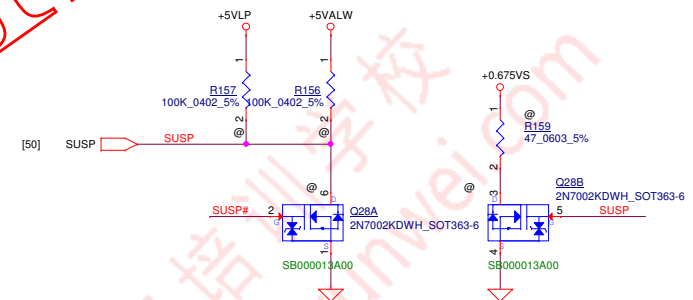
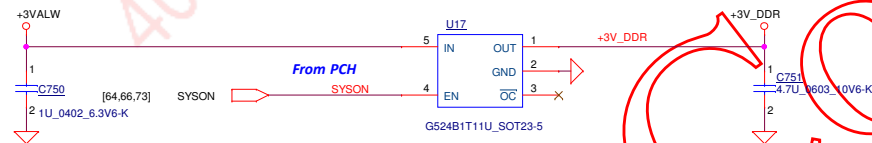
Slew Rate=10uS/V<65uS

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Rev D	Document Number		BR480-NW-A551
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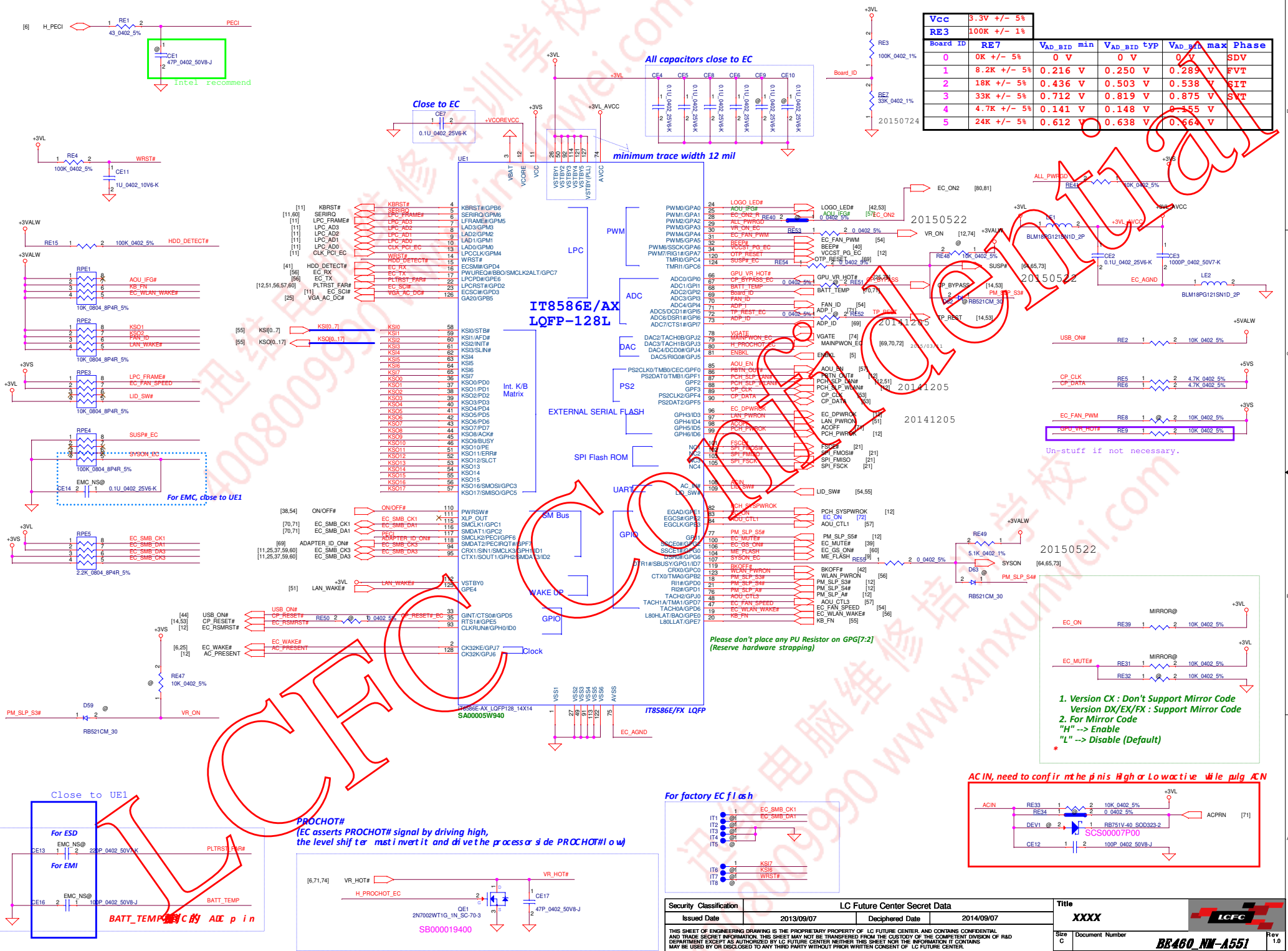
**Load Switch**  
**+5VALW To +5VS**  
**+3VALW To +3VS**



**+3VALW to +3V\_DDR**



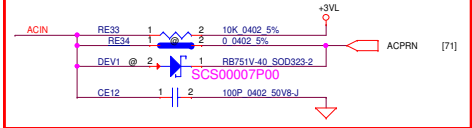
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Issued Date	2013/09/07	Deciphered Date	2014/09/07		
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Vcc	3.3V +/- 5%				
RE3	100K +/- 1%				
Board ID	RE7	VAD_BID min	VAD_BID typ	VAD_BID max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SIT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	STT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	

1. Version CX : Don't Support Mirror Code
  - Version DX/EX/FX : Support Mirror Code
- "H" --> Enable  
"L" --> Disable (Default)


ACIN, need to confir m the pins High or Low active while pulg ACN



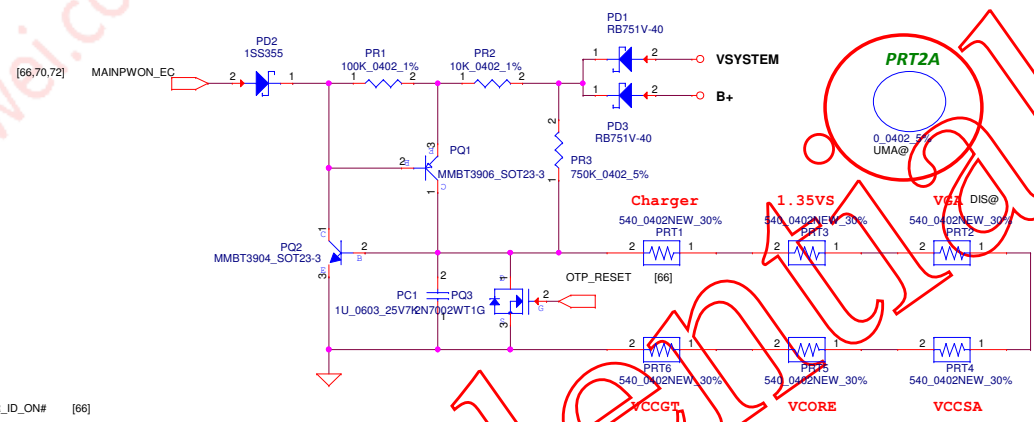
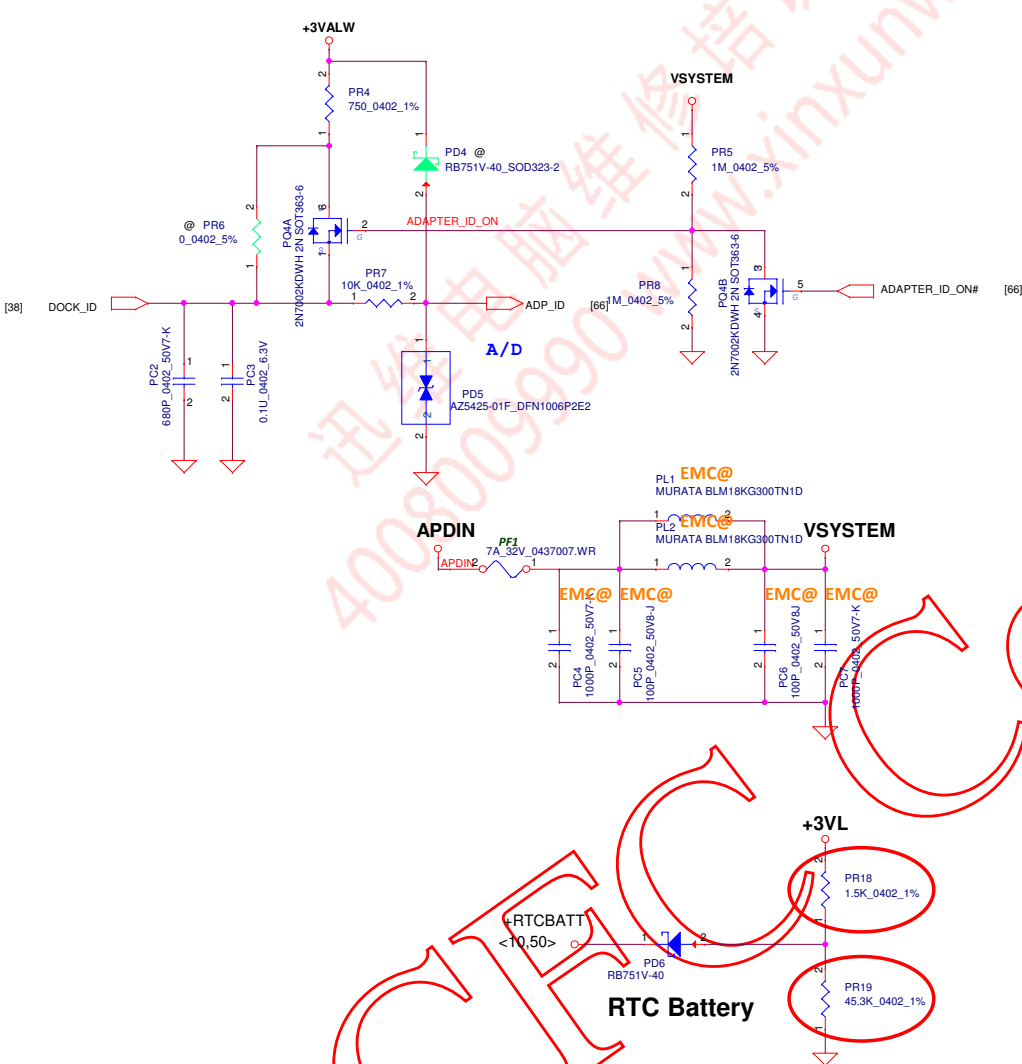
Screw Hole



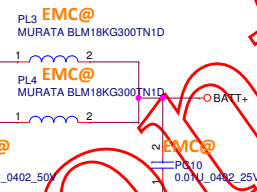
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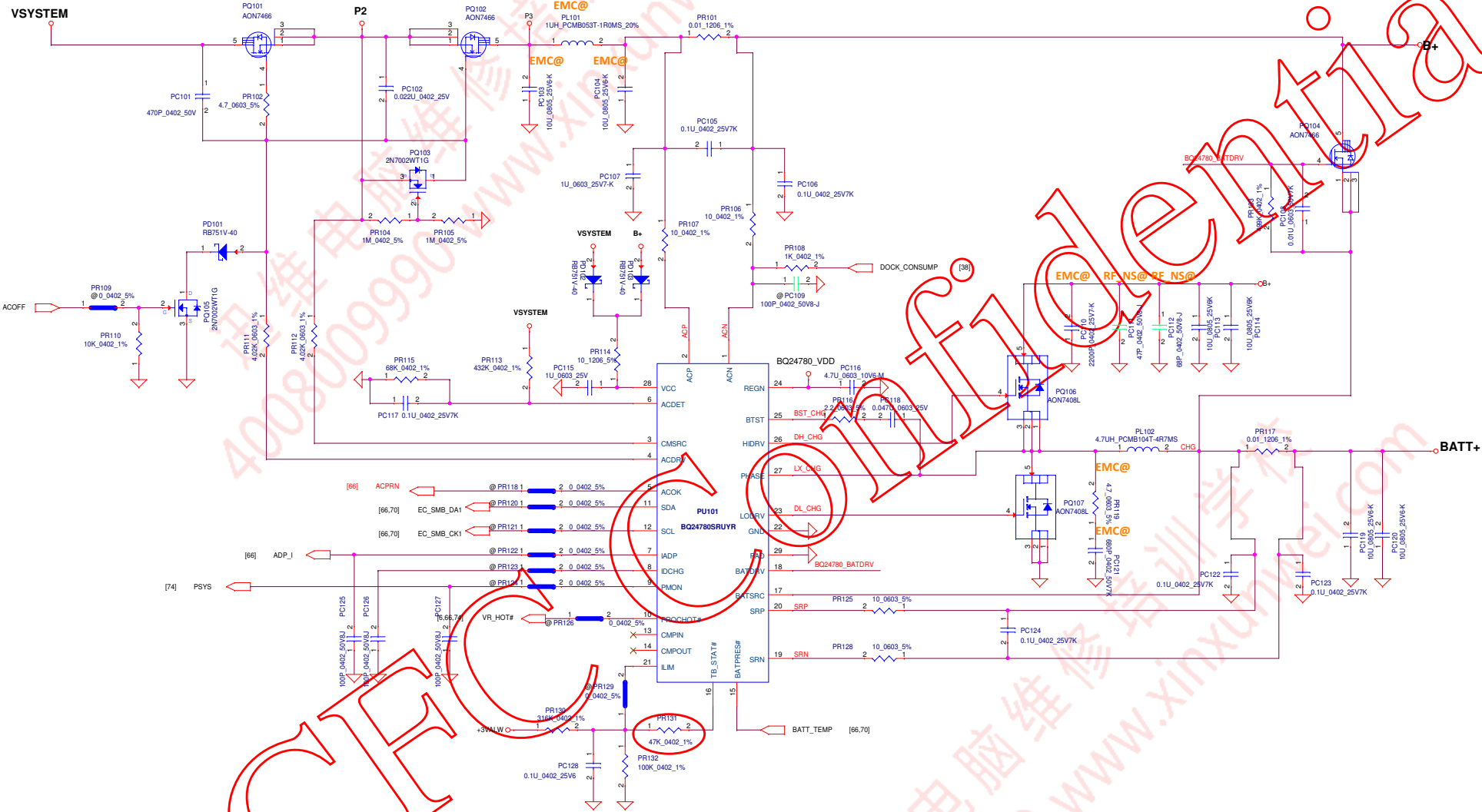
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2013/09/07		2014/09/07					
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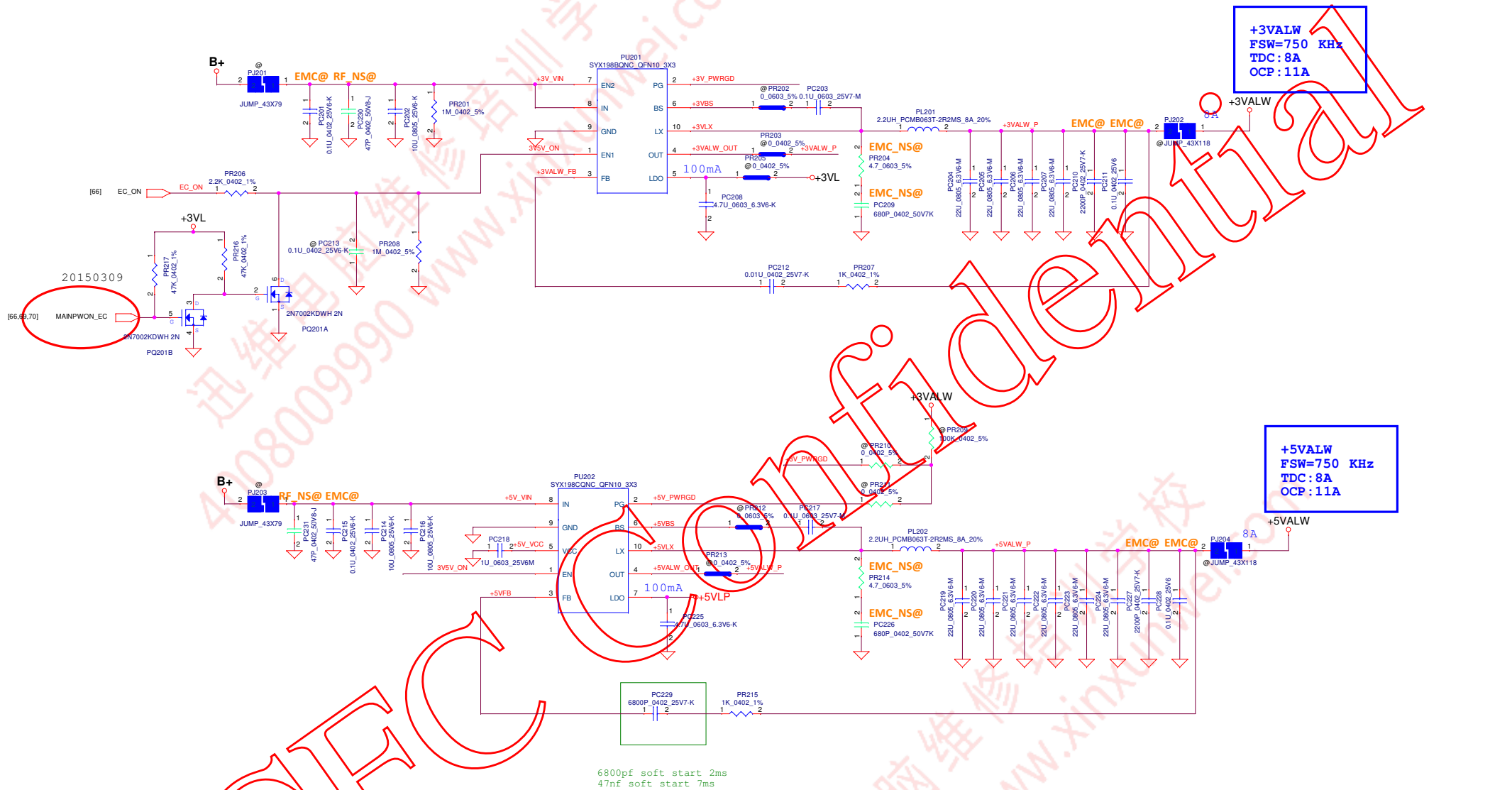




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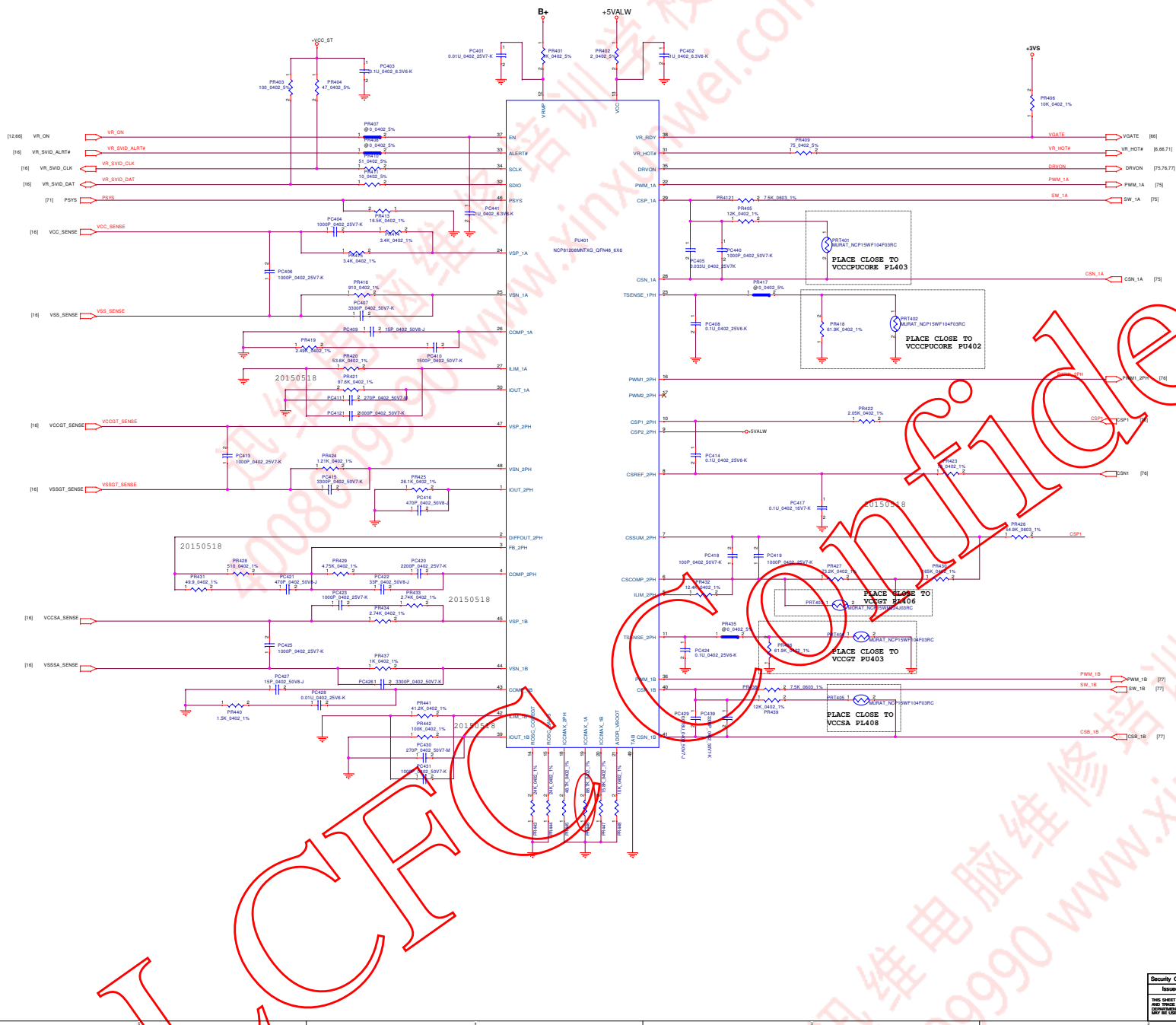


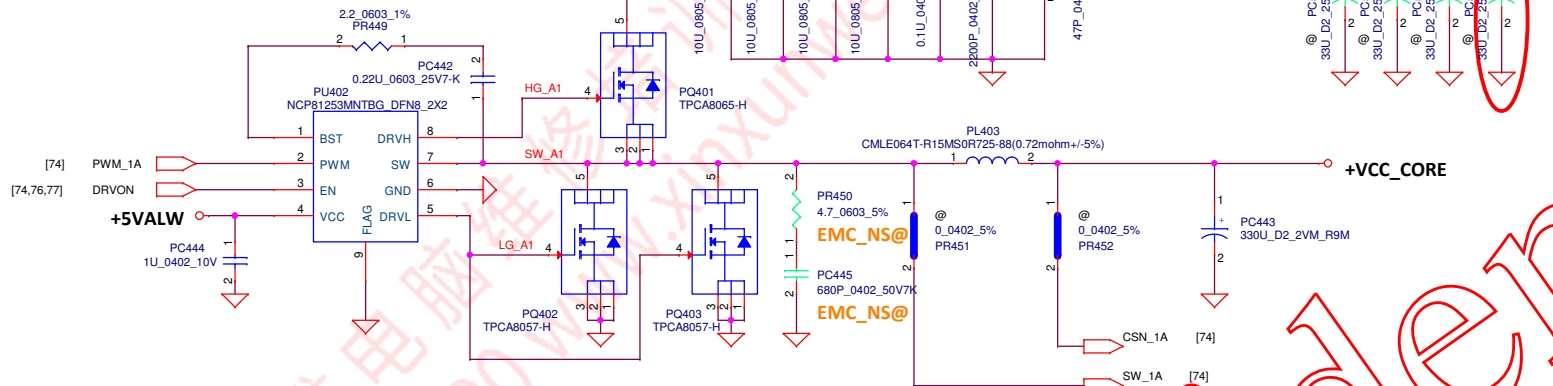


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Issued Date		Deciphered Date		3VALWP/5VALWP	
2013/08/08		2013/08/05		Size	
				Document Number	
				A1VL2 NW-A351	
				Rev	
				1.0	
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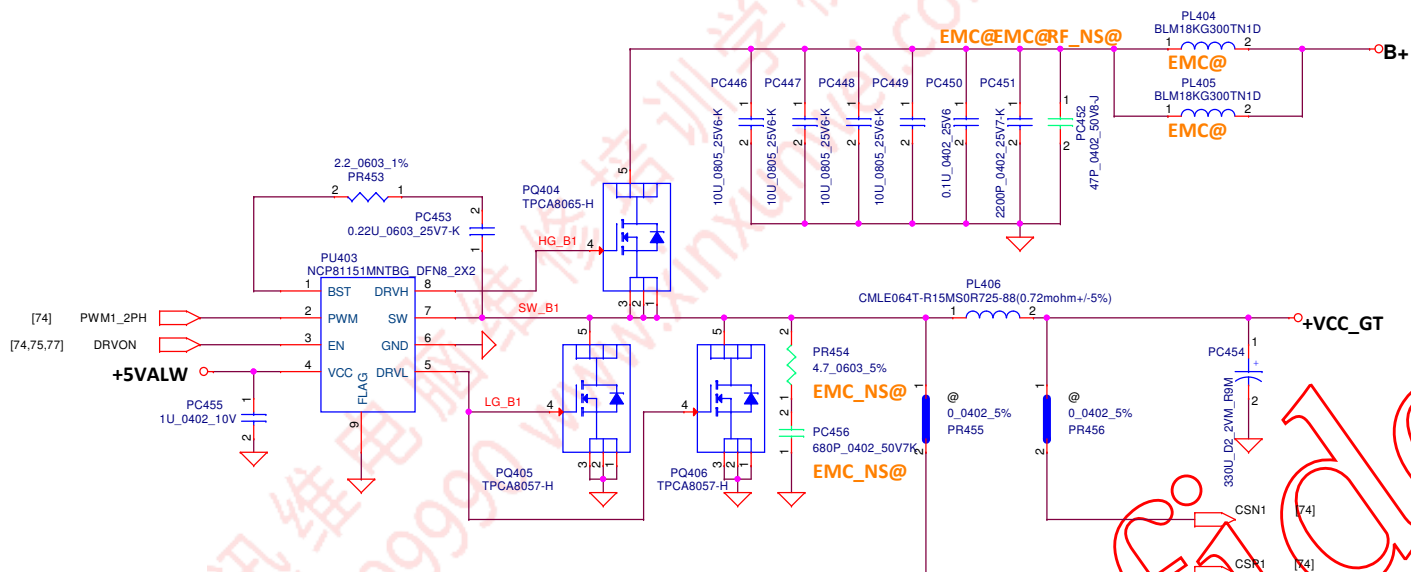






**+VCC\_CORE**  
TDC= 21A  
IccMAX=28A  
OCP = 30A

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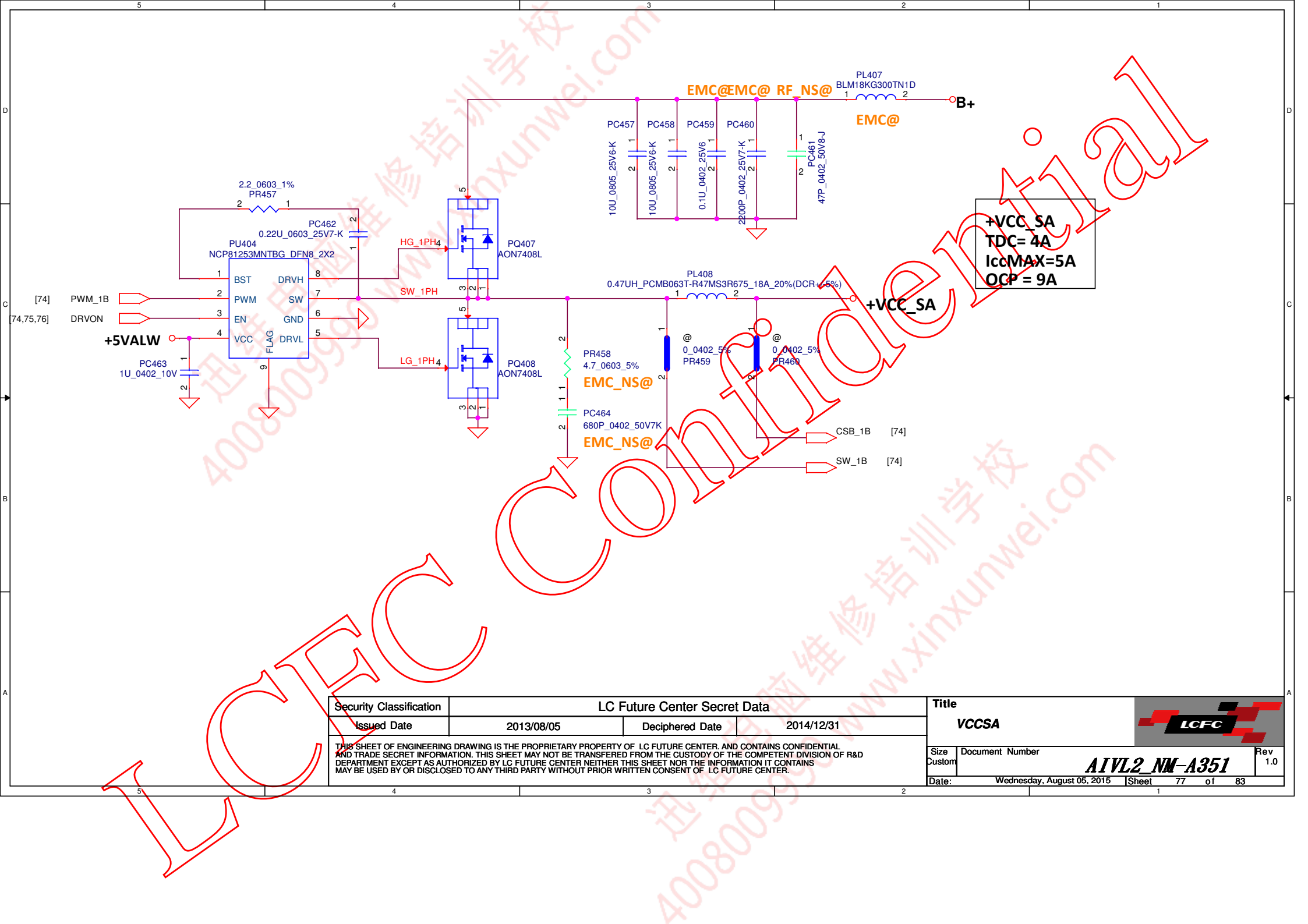


**+VCC\_GT**  
**TDC= 18A**  
**IccMAX=31A**  
**OCP min = 40A**

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Issued Date	2013/08/05	Deciphered Date	2014/12/31

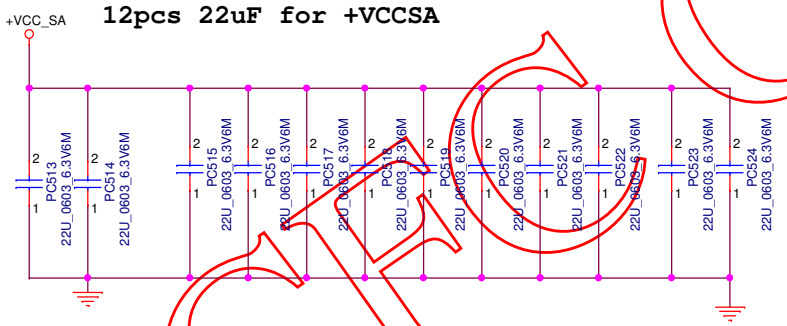
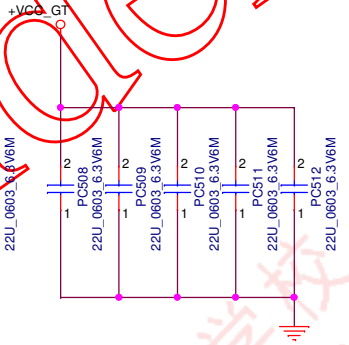
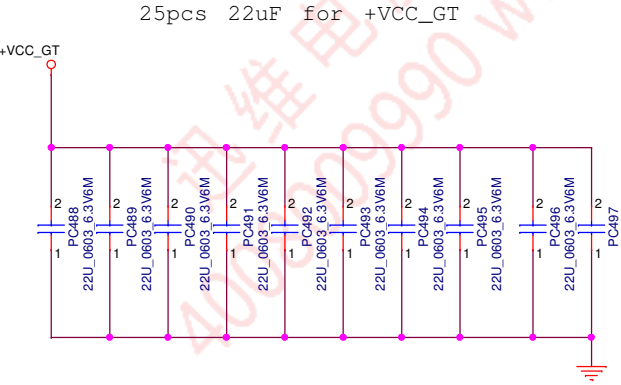
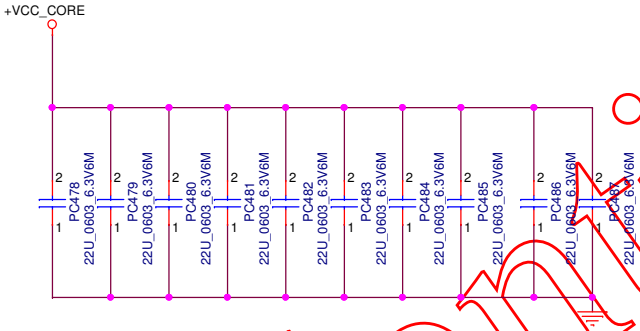
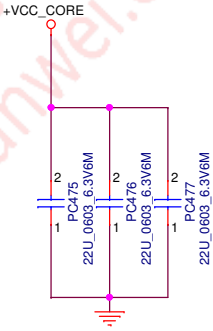
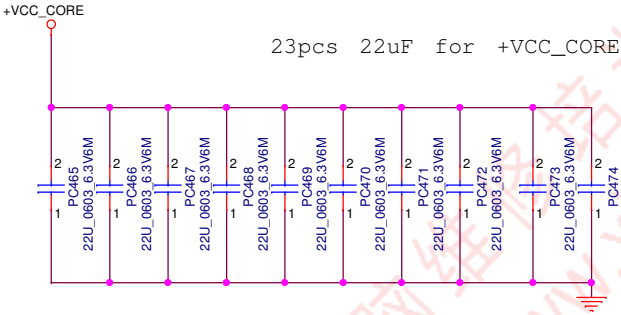
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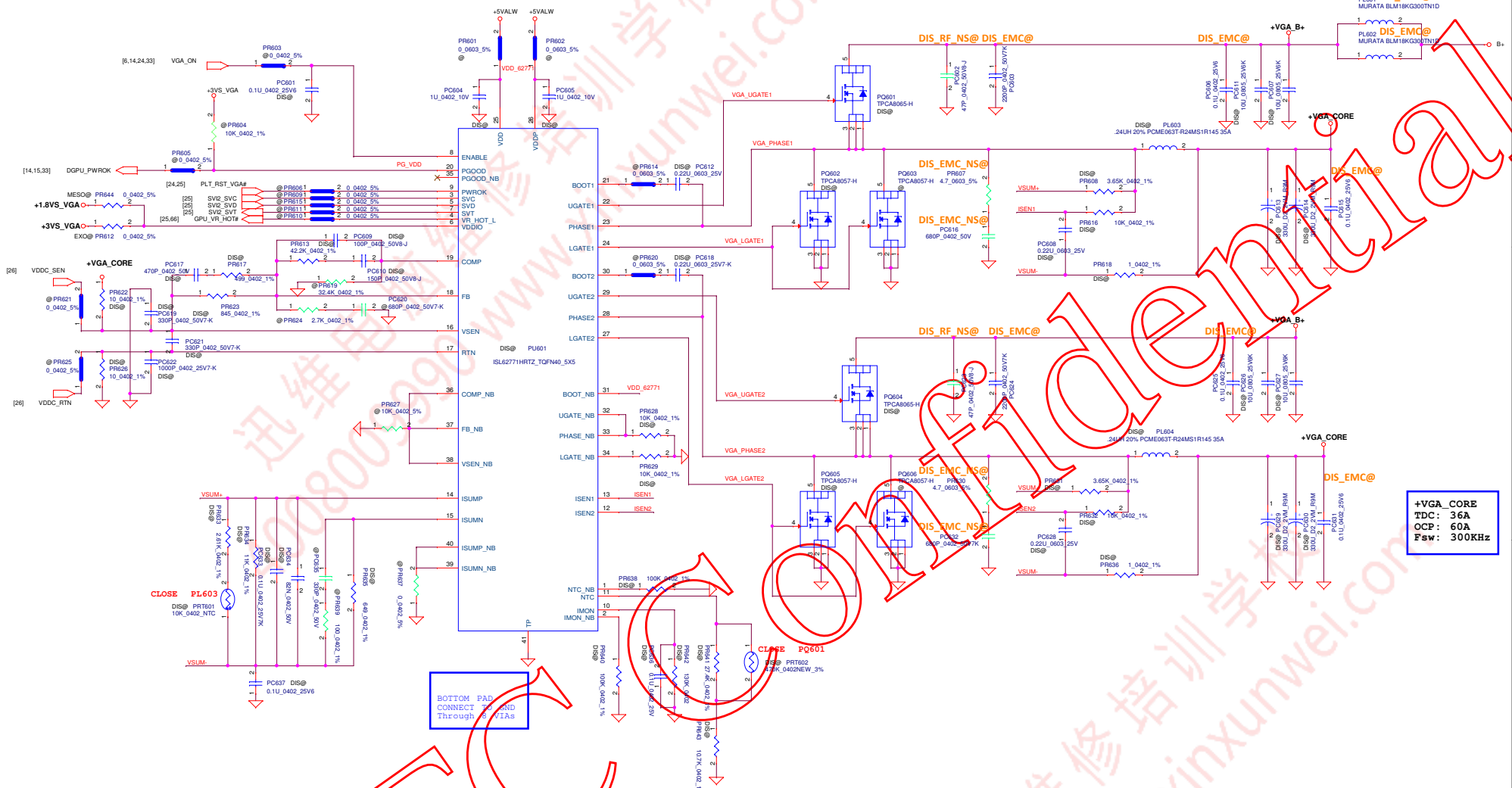


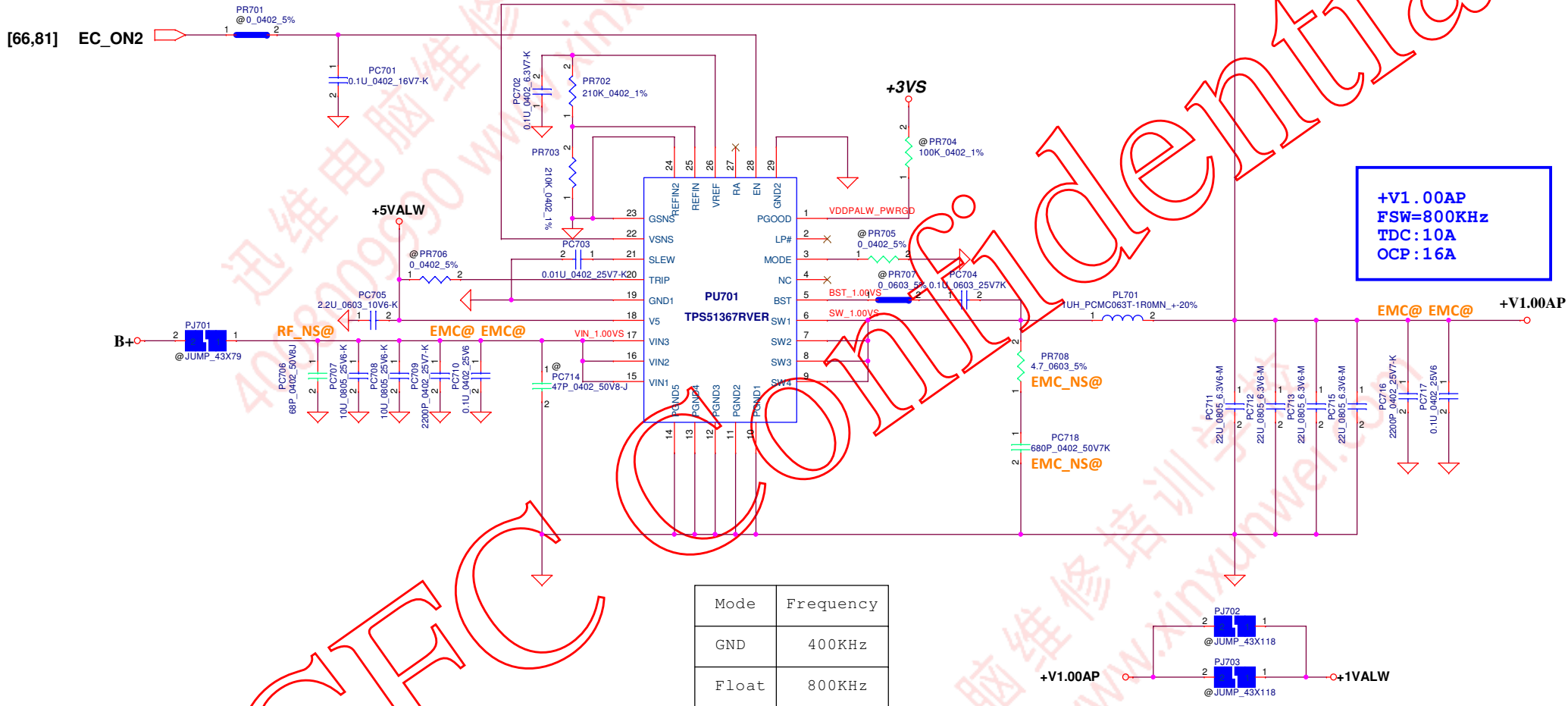
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# ISL62771 Schematic for FT3 solution





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HW PIR (Product Improve Record)

AIVE1 NM-XXXX SCHEMATIC CHANGE LIST  
REVISION CHANGE: 0.1  
GERBER-OUT DATE: 2013/10/15

NO DATE PAGE MODIFICATION LIST PURPOSE

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